S25FL116K

16-Mbit (2-Mbyte) CMOS 3.0-Volt Flash Non-Volatile Memory Serial Peripheral Interface (SPI) with Multi-I/O and Industrial Temperature

Data Sheet *(Advance Information)*

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Publication Number S25FL116K_00 **Revision** 02 **Issue Date** April 10, 2013

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Data Sheet *(Advance Information)*

Features

- **Serial Peripheral Interface (SPI)**
  - SPI Clock polarity and phase modes 0 and 3
  - Command subset and footprint compatible with S25FL016K
- **Read**
  - Normal Read (Serial): 50 MHz clock rate
  - Fast Read (Serial): 108 MHz clock rate
  - Dual / Quad (Multi-I/O) Read 108 MHz clock rate
  - 54 MB/s maximum continuous data transfer rate
  - Efficient eXecute-In-Place (XIP)
    - Continuous and wrapped read modes
  - Serial Flash Discoverable Parameters (SFDP)
- **Program**
  - Serial-input Page Program (up to 256 bytes)
- **Erase**
  - Uniform sector erase (4 kB)
  - Uniform block erase (64 kB)
  - Bulk erase
- **Cycling Endurance**
  - 100K Program-Erase cycles on any sector, minimum
- **Data Retention**
  - 20-year data retention, typical
- **Security**
  - Three 256-byte Security Registers with OTP protection
  - Low supply voltage protection of the entire memory
  - Top / Bottom relative Block Protection Range, 4 kB to all of memory
  - Non-volatile Status Register bits control protection modes
    - Software command protection
    - Hardware input signal protection
    - Lock-Down until power cycle protection
    - OTP protection of security registers
- **90 nm Floating Gate Technology**
- **Single Supply Voltage: 2.7V to 3.6V**
- **Temperature Ranges**
  - Industrial (–40°C to +85°C)
- **Package Options**
  - S25FL116K
    - 8-lead SOIC (150 mil) - SOA008
    - 8-lead SOIC (208 mil) - SOC008
    - 8-contact USON 5x6 - WND008
    - 24-ball BGA 6 mm x 8 mm - FAB024 and FAC024
    - KGD/KGW

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1. Performance Summary

Table 1.1 Maximum Read Rates (V_{CC} = 2.7V to 3.6V, 105°C)

Command	Clock Rate (MHz)	Mbytes/s
Read	50	6
Fast Read	108	13.5
Dual Read	108	27
Quad Read	108	54

Table 1.2 Typical Program and Erase Rates (V_{CC} = 2.7V to 3.6V, 105°C)

Operation	kbytes/s
Page Programming (256-byte page buffer)	365
4-kbyte Sector Erase	58
64-kbyte Sector Erase	187

Table 1.3 Typical Current Consumption (V_{CC} = 2.7V to 3.6V, 105°C)

Operation	Current (mA)
Serial Read 50 MHz	7
Serial Read 108 MHz	12
Dual Read 108 MHz	14
Quad Read 108 MHz	16
Program	20
Erase	20
Standby	0.020
Deep Power Down	0.002

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2. General Description

The S25FL116K of the FL1-K family non-volatile flash memory devices connect to a host system via a Serial Peripheral Interface (SPI). Traditional SPI single bit serial input and output (SIngle I/O or SIO) is supported as well as optional two bit (Dual I/O or DIO) and four bit (Quad I/O or QIO) serial protocols. This multiple width interface is called SPI Multi-I/O or MIO.

The SPI-MIO protocols use only 4 to 6 signals:

- Chip Select (CS#)
- Serial Clock (CLK)
- Serial Data
  - IO0 (SI)
  - IO1 (SO)
  - IO2 (WP#)
  - IO3 (HOLD#)

The SIO protocol uses Serial Input (SI) and Serial Output (SO) for data transfer. The DIO protocols use IO0 and IO1 to input or output two bits of data in each clock cycle.

The Write Protect (WP#) input signal option allows hardware control over data protection. Software controlled commands can also manage data protection.

The QIO protocols use all of the data signals (IO0 to IO3) to transfer 4 bits in each clock cycle. When the QIO protocols are enabled the WP# and HOLD# inputs and features are disabled.

Clock frequency of up to 108 MHz is supported, allowing data transfer rates up to:

- Single bit data path = 13.5 Mbytes/s
- Dual bit data path = 27 Mbytes/s
- Quad bit data path = 54 Mbytes/s

Executing code directly from flash memory is often called eXecute-In-Place or XIP. By using S25FL116K devices at the higher clock rates supported, with QIO commands, the command read transfer rate can match or exceed traditional x8 or x16 parallel interface, asynchronous, NOR flash memories, while reducing signal count dramatically. The Continuous Read Mode allows for random memory access with as few as 8-clocks of overhead for each access, providing efficient XIP operation. The Wrapped Read mode provides efficient instruction or data cache refill via a fast read of the critical byte that causes a cache miss, followed by reading all other bytes in the same cache line in a single read command.

The S25FL116K:

- Support JEDEC standard manufacturer and device type identification.
- Program pages of 256 bytes each. One to 256 bytes can be programmed in each Page Program operation. Pages can be erased in groups of 16 (4-kB aligned sector erase), groups of 256 (64-kB aligned block erase), or the entire chip (chip erase).
- The S25FL116K operates on a single 2.7V to 3.6V power supply and all devices are offered in space-saving packages.
- Provides an ideal storage solution for systems with limited space, signal connections, and power. These memories offer flexibility and performance well beyond ordinary serial flash devices. They are ideal for code shadowing to RAM, executing code directly (XIP), and storing reprogrammable data.

2.1 Migration Notes

2.1.1 Features Comparison

The S25FL1-K (S25FL116K, S25FL132K, and S25FL164K) is command set and footprint compatible with prior generation FL-K and FL-P families.

Table 2.1 FL Generations Comparison

Parameter	S25FL1-K	S25FL-K	S25FL-P
Technology Node	90 nm	90 nm	90 nm
Architecture	Floating Gate	Floating Gate	MirrorBit®
Release Date	1H2013	In Production	In Production
Density	16 Mbit - 64 Mbit	4 Mbit - 128 Mbit	32 Mbit - 256 Mbit
Bus Width	x1, x2, x4	x1, x2, x4	x1, x2, x4
Supply Voltage	2.7V - 3.6V	2.7V - 3.6V	2.7V - 3.6V
Normal Read Speed	6 MB/s (50 MHz)	6 MB/s (50 MHz)	5 MB/s (40 MHz)
Fast Read Speed	13.5 MB/s (108 MHz)	13 MB/s (104 MHz)	13 MB/s (104 MHz)
Dual Read Speed	27 MB/s (108 MHz)	26 MB/s (104 MHz)	20 MB/s (80 MHz)
Quad Read Speed	54 MB/s (108 MHz)	52 MB/s (104 MHz)	40 MB/s (80 MHz)
Program Buffer Size	256B	256B	256B
Page Programming Time (typ.)	700 µs (256B)	700 µs (256B)	1500 µs (256B)
Program Suspend/Resume	No	Yes	No
Erase Sector Size	4 kB / 64 kB	4 kB / 32 kB / 64 kB	64 kB / 256 kB
Parameter Sector Size	N/A	N/A	4 kB
Sector Erase Time (typ.)	70 ms (4 kB), 350 ms (64 kB)	30 ms (4 kB), 150 ms (64 kB)	500 ms (64 kB)
Erase Suspend/Resume	No	Yes	No
OTP Size	768B (3 x 256B)	768B (3 x 256B)	506B
Operating Temperature	–40°C to +85°C	–40°C to +85°C	–40°C to +85°C/+105°C

Notes:

1. *S25FL-K family devices can erase 4-kB sectors in groups of 32 kB or 64 kB.*
2. *S25FL1-K family devices can erase 4-kB sectors in groups of 64 kB.*
3. *S25FL-P has either 64-kB or 256-kB uniform sectors depending on an ordering option.*
4. *Refer to individual data sheets for further details.*

2.1.2 Known Feature Differences from Prior Generations

2.1.2.1 Secure Silicon Region (OTP)

The size and format (address map) of the One Time Program area is the same for the S25FL1-K and the S25FL-K but different for the S25FL-P.

2.1.2.2 Commands Not Supported

The following S25FL-K and S25FL-P commands are not supported:

- Quad Page PGM (32h)
- Half-Block Erase 32K (52h)
- Word read Quad I/O (E7)
- Octal Word Read Quad I/O (E3h)
- MFID dual I/O (92h)
- MFID quad I/O (94h)
- Read Unique ID (4Bh)

2.1.2.3 New Features

The S25FL116K introduces new features to low density SPI category memories:

- Variable read latency (number of dummy cycles) for faster initial access time or higher clock rate read commands
- Volatile configuration option in addition to legacy non-volatile configuration

2.2 Glossary

- **Command** = All information transferred between the host system and memory during one period while CS# is low. This includes the instruction (sometimes called an operation code or opcode) and any required address, mode bits, latency cycles, or data.
- **Flash** = The name for a type of Electrical Erase Programmable Read Only Memory (EEPROM) that erases large blocks of memory bits in parallel, making the erase operation much faster than early EEPROM.
- **High** = A signal voltage level ≥ V_{IH} or a logic level representing a binary one (1).
- **Instruction** = The 8-bit code indicating the function to be performed by a command (sometimes called an operation code or opcode). The instruction is always the first 8 bits transferred from host system to the memory in any command.
- **Low** = A signal voltage level ≤ V_{IL} or a logic level representing a binary zero (0).
- **LSB** = Least Significant Bit = Generally the right most bit, with the lowest order of magnitude value, within a group of bits of a register or data value.
- **MSB** = Most Significant Bit = Generally the left most bit, with the highest order of magnitude value, within a group of bits of a register or data value.
- **Non-Volatile** = No power is needed to maintain data stored in the memory.
- **OPN** = Ordering Part Number = The alphanumeric string specifying the memory device type, density, package, factory non-volatile configuration, etc. used to select the desired device.
- **Page** = 256-byte aligned and length group of data.
- **PCB =** Printed Circuit Board.
- **Register Bit References** = Are in the format: Register_name[bit_number] or Register_name[bit_range_MSB: bit_range_LSB].
- **Sector** = Erase unit size; all sectors are physically 4-kbytes aligned and length. Depending on the erase command used, groups of physical sectors may be erased as a larger logical sector of 64 kbytes.
- **Write** = An operation that changes data within volatile or non-volatile registers bits or non-volatile flash memory. When changing non-volatile data, an erase and reprogramming of any unchanged non-volatile data is done, as part of the operation, such that the non-volatile data is modified by the write operation, in the same way that volatile data is modified – as a single operation. The non-volatile data appears to the host system to be updated by the single write command, without the need for separate commands for erase and reprogram of adjacent, but unaffected data.

2.3 Other Resources

2.3.1 Links to Software

http://www.spansion.com/Support/Pages/Support.aspx

2.3.2 Links to Application Notes

http://www.spansion.com/Support/TechnicalDocuments/Pages/ApplicationNotes.aspx

2.3.3 Specification Bulletins

Specification bulletins provide information on temporary differences in feature description or parametric variance since the publication of the last full data sheet. Contact your local sales office for details. Obtain the latest list of company locations and contact information at:

http://www.spansion.com/About/Pages/Locations.aspx

Hardware Interface

Serial Peripheral Interface with Multiple Input / Output (SPI-MIO)

Many memory devices connect to their host system with separate parallel control, address, and data signals that require a large number of signal connections and larger package size. The large number of connections increase power consumption due to so many signals switching and the larger package increases cost.

The S25FL116K reduces the number of signals for connection to the host system by serially transferring all control, address, and data information over 4 to 6 signals. This reduces the cost of the memory package, reduces signal switching power, and either reduces the host connection count or frees host connectors for use in providing other features.

The S25FL116K uses the industry standard single bit Serial Peripheral Interface (SPI) and also supports commands for two bit (Dual) and four bit (Quad) wide serial transfers. This multiple width interface is called SPI Multi-I/O or SPI-MIO.

3. Signal Descriptions

3.1 Input/Output Summary

Table 3.1 Signal List

Signal Name	Type	Description
SCK	Input	**Serial Clock.**
CS#	Input	**Chip Select.**
SI (IO0)	I/O	**Serial Input** for single bit data commands. IO0 for Dual or Quad commands.
SO (IO1)	I/O	**Serial Output** for single bit data commands. IO1 for Dual or Quad commands.
WP# (IO2)	I/O	**Write Protect** in single bit or Dual data commands. IO2 in Quad mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
HOLD# (IO3)	I/O	**Hold** (pause) serial transfer in single bit or Dual data commands. IO3 in Quad-I/O mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
V_{CC}	Supply	**Core and I/O Power Supply.**
V_{SS}	Supply	**Ground.**
NC	Unused	**Not Connected.** No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). However, any signal connected to an NC must not have voltage levels higher than V_{CC}.
RFU	Reserved	**Reserved for Future Use.** No device internal signal is currently connected to the package connector but there is potential future use of the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.
DNU	Reserved	**Do Not Use.** A device internal signal may be connected to the package connector. The connection may be used by Spansion® for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to this connection.

Note:

1. A signal name ending with the # symbol is active when low.

3.2 Address and Data Configuration

Traditional SPI single bit wide commands (Single or SIO) send information from the host to the memory only on the SI signal. Data may be sent back to the host serially on the Serial Output (SO) signal.

Dual or Quad Output commands send information from the host to the memory only on the SI signal. Data will be returned to the host as a sequence of bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

Dual or Quad Input / Output (I/O) commands send information from the host to the memory as bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

3.3 Serial Clock (SCK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCK signal. Data output changes after the falling edge of SCK.

3.4 Chip Select (CS#)

The chip select signal indicates when a command for the device is in process and the other signals are relevant for the memory device. When the CS# signal is at the logic high state, the device is not selected and all input signals are ignored and all output signals are high impedance. Unless an internal Program, Erase or Write Status Registers embedded operation is in progress, the device will be in the Standby Power mode. Driving the CS# input to logic low state enables the device, placing it in the Active Power mode. After Power-up, a falling edge on CS# is required prior to the start of any command.

3.5 Serial Input (SI) / IO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCK clock signal.

SI becomes IO0 - an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK).

3.6 Serial Output (SO) / IO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCK clock signal.

SO becomes IO1—an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK).

3.7 Write Protect (WP#) / IO2

When WP# is driven Low (V_{IL}), while the Status Register Protect bits (SRP1 and SRP0) of the Status Registers (SR2[0] and SR1[7]) are set to 0 and 1 respectively, it is not possible to write to the Status Registers. This prevents any alteration of the Status Registers. As a consequence, all the data bytes in the memory area that are protected by the Block Protect, TB, SEC, and CMP bits in the Status Registers, are also hardware protected against data modification while WP# remains Low.

The WP# function is not available when the Quad mode is enabled (QE) in Status Register-2 (SR2[1]=1). The WP# function is replaced by IO2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK).

WP# has an internal pull-up resistance; when unconnected, WP# is at V_{IH} and may be left unconnected in the host system if not used for Quad mode.

3.8 HOLD# / IO3

The HOLD# signal is used to pause any serial communications with the device without deselecting the device or stopping the serial clock.

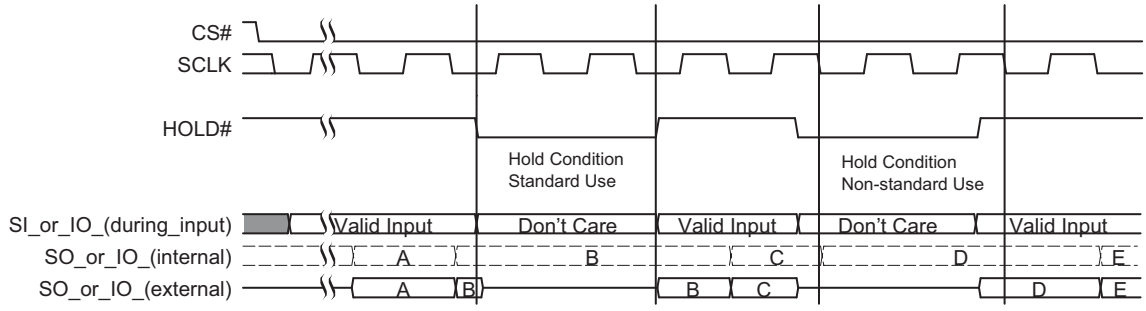
To enter the Hold condition, the device must be selected by driving the CS# input to the logic low state. It is required that the user keep the CS# input low state during the entire duration of the Hold condition. This is to ensure that the state of the interface logic remains unchanged from the moment of entering the Hold condition.

The Hold condition starts on the falling edge of the Hold (HOLD#) signal, provided that this coincides with SCK being at the logic low state. If the falling edge does not coincide with the SCK signal being at the logic low state, the Hold condition starts whenever the SCK signal reaches the logic low state. Taking the HOLD# signal to the logic low state does not terminate any Write, Program or Erase operation that is currently in progress.

During the Hold condition, SO is in high impedance and both the SI and SCK input are Don't Care.

The Hold condition ends on the rising edge of the Hold (HOLD#) signal, provided that this coincides with the SCK signal being at the logic low state. If the rising edge does not coincide with the SCK signal being at the logic low state, the Hold condition ends whenever the SCK signal reaches the logic low state.

Figure 3.1 Hold Condition



3.9 Core and I/O Signal Voltage Supply (V_{CC})

V_{CC} is the voltage source for all device internal logic and input/output signals. It is the single voltage used for all device functions including read, program, and erase.

3.10 Supply and Signal Ground (V_{SS})

V_{SS} is the common voltage drain and ground reference for the device core, input signal receivers, and output drivers.

3.11 Not Connected (NC)

No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB).

3.12 Reserved for Future Use (RFU)

No device internal signal is currently connected to the package connector but is there potential future use for the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.

3.13 Do Not Use (DNU)

A device internal signal may be connected to the package connector. The connection may be used by Spansion for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections.

3.14 Block Diagrams

Figure 3.2 Bus Master and Memory Devices on the SPI Bus - Single Bit Data Path

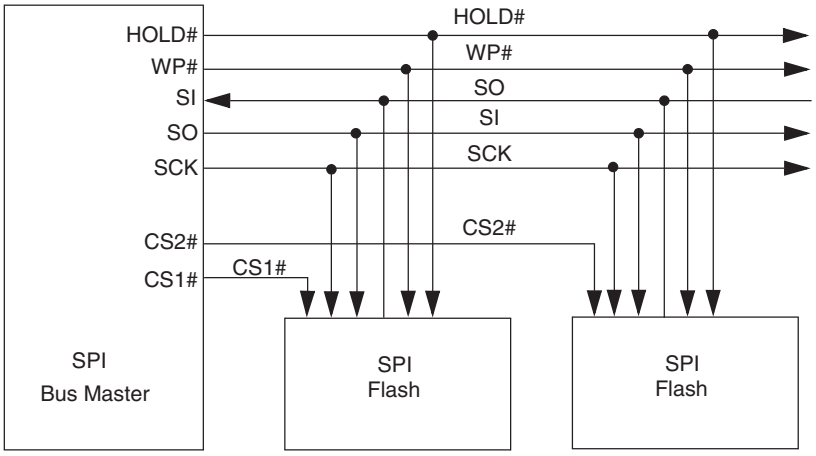


Figure 3.3 Bus Master and Memory Devices on the SPI Bus - Dual Bit Data Path

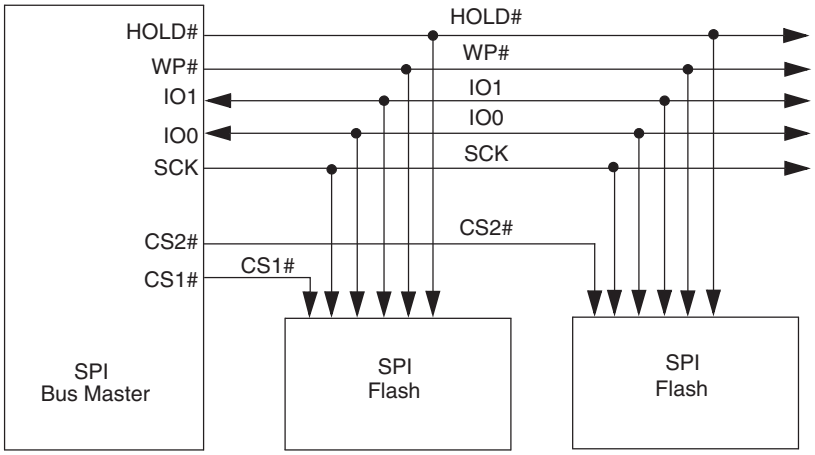
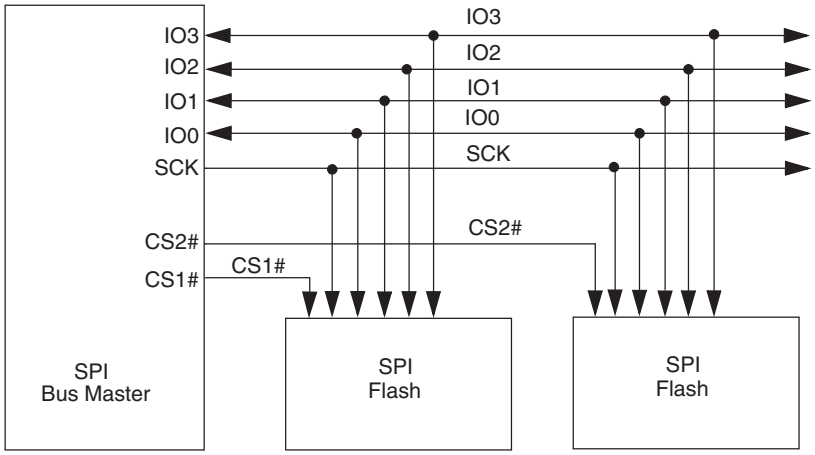


Figure 3.4 Bus Master and Memory Devices on the SPI Bus - Quad Bit Data Path



4. Signal Protocols

4.1 SPI Clock Modes

The S25FL116K can be driven by an embedded microcontroller (bus master) in either of the two following clocking modes.

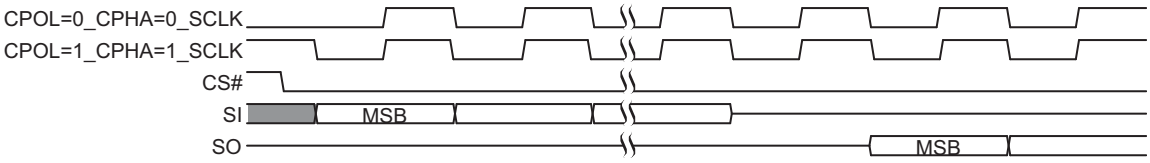
- **Mode 0** with Clock Polarity (CPOL) = 0 and, Clock Phase (CPHA) = 0
- **Mode 3** with CPOL = 1 and, CPHA = 1

For these two modes, input data into the device is always latched in on the rising edge of the SCK signal and the output data is always available from the falling edge of the SCK clock signal.

The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring any data.

- SCK will stay at logic low state with CPOL = 0, CPHA = 0
- SCK will stay at logic high state with CPOL = 1, CPHA = 1

Figure 4.1 SPI Modes Supported



Timing diagrams throughout the remainder of the document are generally shown as both mode 0 and 3 by showing SCLK as both high and low at the fall of CS#. In some cases a timing diagram may show only mode 0 with SCLK low at the fall of CS#. In such a case, mode 3 timing simply means clock is high at the fall of CS# so no SCLK rising edge set up or hold time to the falling edge of CS# is needed for mode 3.

SCLK cycles are measured (counted) from one falling edge of SCLK to the next falling edge of SCLK. In mode 0 the beginning of the first SCLK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCLK because SCLK is already low at the beginning of a command.

4.2 Command Protocol

All communication between the host system and S25FL116K is in the form of units called commands.

All commands begin with an instruction that selects the type of information transfer or device operation to be performed. Commands may also have an address, instruction modifier (mode), latency period, data transfer to the memory, or data transfer from the memory. All instruction, address, and data information is transferred serially between the host system and memory device.

All instructions are transferred from host to memory as a single bit serial sequence on the SI signal.

Single bit wide commands may provide an address or data sent only on the SI signal. Data may be sent back to the host serially on the SO signal.

Dual or Quad Output commands provide an address sent to the memory only on the SI signal. Data will be returned to the host as a sequence of bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

Dual or Quad Input / Output (I/O) commands provide an address sent from the host as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3.

Commands are structured as follows:

- Each command begins with CS# going low and ends with CS# returning high. The memory device is selected by the host driving the Chip Select (CS#) signal low throughout a command.

- The serial clock (SCK) marks the transfer of each bit or group of bits between the host and memory.
- Each command begins with an eight bit (byte) instruction. The instruction is always presented only as a single bit serial sequence on the Serial Input (SI) signal with one bit transferred to the memory device on each SCK rising edge. The instruction selects the type of information transfer or device operation to be performed.
- The instruction may be stand alone or may be followed by address bits to select a location within one of several address spaces in the device. The instruction determines the address space used. The address is a 24-bit, byte boundary, address. The address transfers occur on SCK rising edge.
- The width of all transfers following the instruction are determined by the instruction sent. Following transfers may continue to be single bit serial on only the SI or Serial Output (SO) signals, they may be done in 2-bit groups per (dual) transfer on the IO0 and IO1 signals, or they may be done in 4-bit groups per (quad) transfer on the IO0-IO3 signals. Within the dual or quad groups the least significant bit is on IO0. More significant bits are placed in significance order on each higher numbered IO signal. SIngle bits or parallel bit groups are transferred in most to least significant bit order.
- Some instructions send an instruction modifier called mode bits, following the address, to indicate that the next command will be of the same type with an implied, rather than an explicit, instruction. The next command thus does not provide an instruction byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands. The mode bit transfers occur on SCK rising edge.
- The address or mode bits may be followed by write data to be stored in the memory device or by a read latency period before read data is returned to the host.
- Write data bit transfers occur on SCK rising edge.
- SCK continues to toggle during any read access latency period. The latency may be zero to several SCK cycles (also referred to as dummy cycles). At the end of the read latency cycles, the first read data bits are driven from the outputs on SCK falling edge at the end of the last read latency cycle. The first read data bits are considered transferred to the host on the following SCLK rising edge. Each following transfer occurs on the next SCK rising edge.
- If the command returns read data to the host, the device continues sending data transfers until the host takes the CS# signal high. The CS# signal can be driven high after any transfer in the read data sequence. This will terminate the command.
- At the end of a command that does not return data, the host drives the CS# input high. The CS# signal must go high after the eighth bit, of a stand alone instruction or, of the last write data byte that is transferred. That is, the CS# signal must be driven high when the number of clock cycles after CS# signal was driven low is an exact multiple of eight cycles. If the CS# signal does not go high exactly at the eight SCLK cycle boundary of the instruction or write data, the command is rejected and not executed.
- All instruction, address, and mode bits are shifted into the device with the Most Significant Bits (MSB) first. The data bits are shifted in and out of the device MSB first. All data is transferred in byte units with the lowest address byte sent first. Following bytes of data are sent in lowest to highest byte address order i.e. the byte address increments.
- All attempts to read the flash memory array during a program, erase, or a write cycle (embedded operations) are ignored. The embedded operation will continue to execute without any affect. A very limited set of commands are accepted during an embedded operation. These are discussed in the individual command descriptions.
- Depending on the command, the time for execution varies. A command to read status information from an executing command is available to determine when the command completes execution and whether the command was successful.

4.2.1 Command Sequence Examples

Figure 4.2 Stand Alone Instruction Command

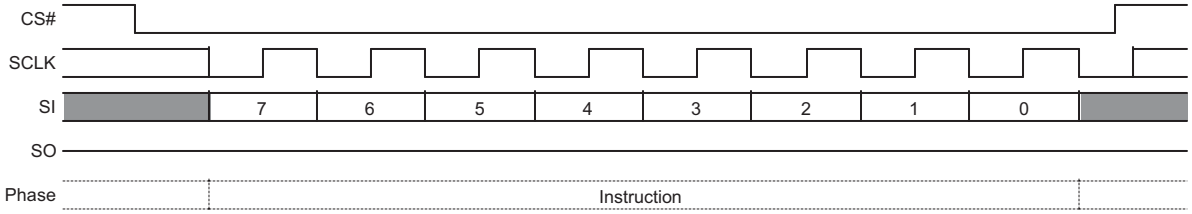


Figure 4.3 Single Bit Wide Input Command

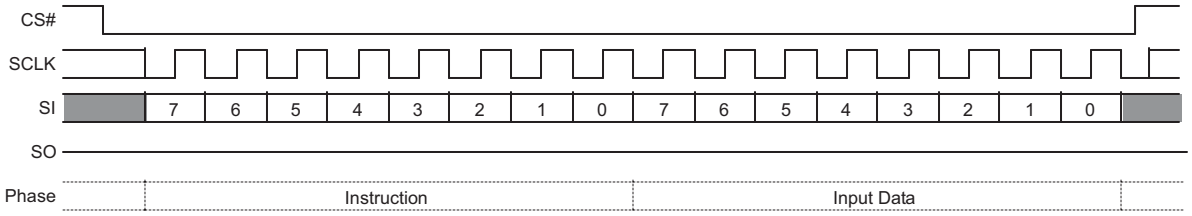


Figure 4.4 Single Bit Wide Output Command

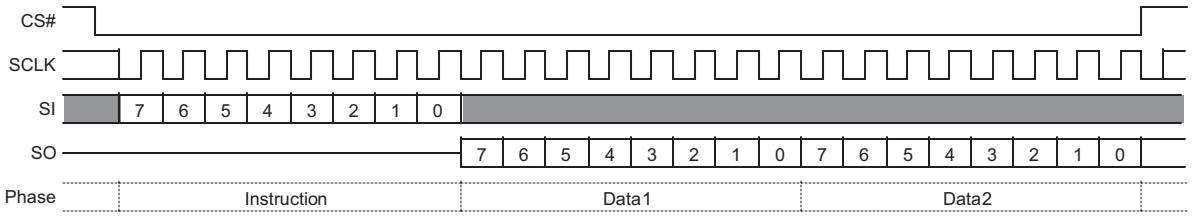


Figure 4.5 Single Bit Wide I/O Command without Latency

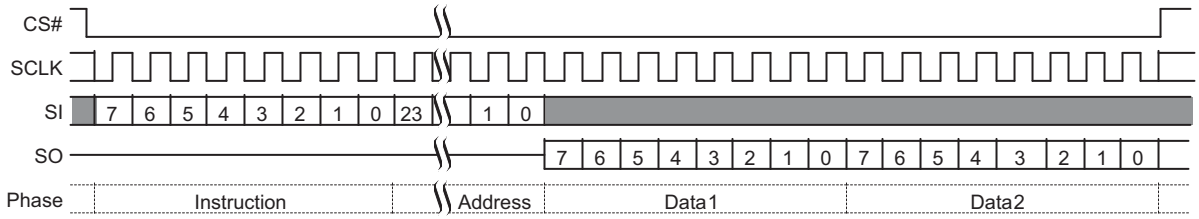


Figure 4.6 Single Bit Wide I/O Command with Latency

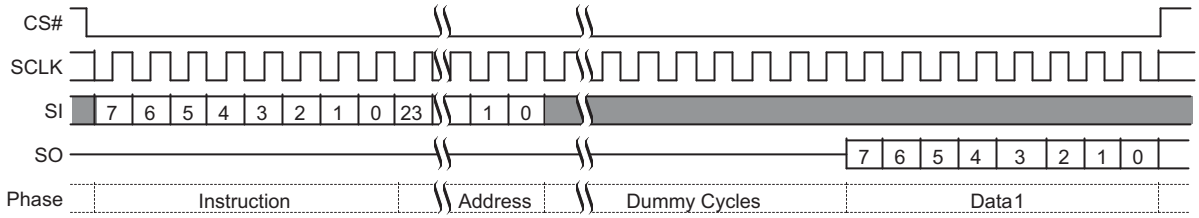


Figure 4.7 Dual Output Command

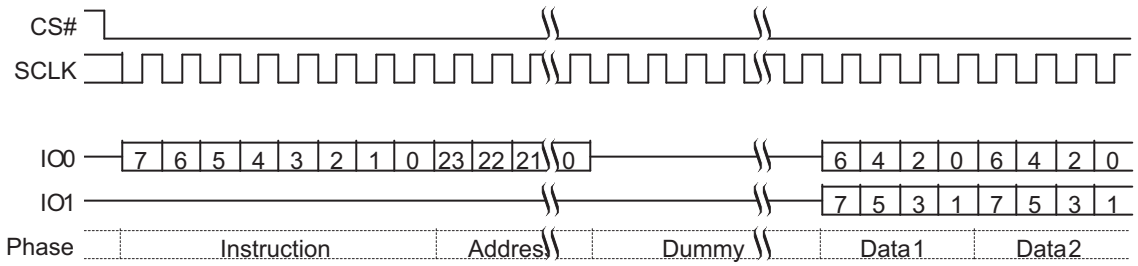


Figure 4.8 Quad Output Command without Latency

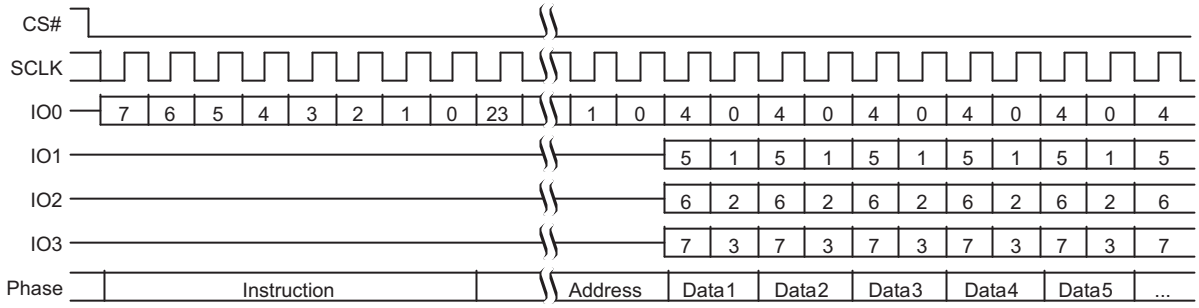


Figure 4.9 Dual I/O Command

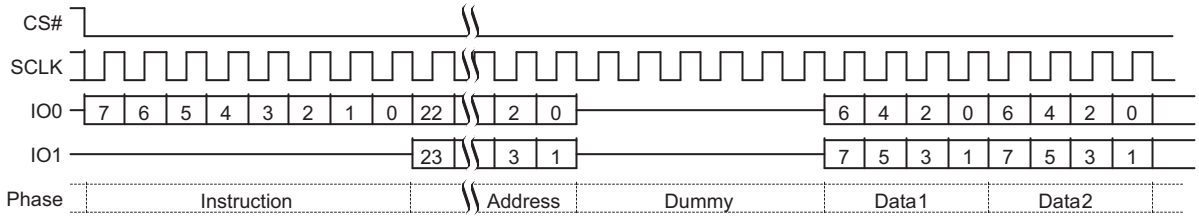
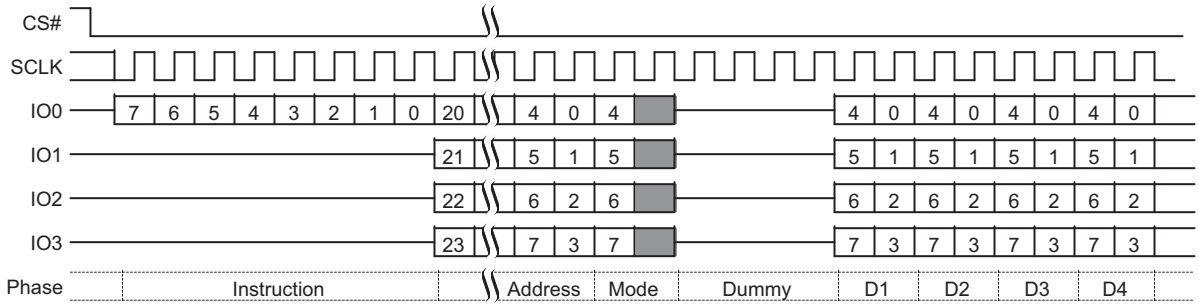


Figure 4.10 Quad I/O Command



Additional sequence diagrams, specific to each command, are provided in *Commands* on page 53

4.3 Interface States

This section describes the input and output signal levels as related to the SPI interface behavior.

Table 4.1 Interface States Summary

Interface State	V_{CC}	SCLK	CS#	HOLD# / IO3	WP# / IO2	SO / IO1	SI / IO0
Low Power Hardware Data Protection	< V_{WI}	X	X	X	X	Z	X
Power-On (Cold) Reset	≥ V_{CC} (min)	X	HH	X	X	Z	X
Interface Standby	≥ V_{CC} (min)	X	X	X	X	Z	X
Instruction Cycle	≥ V_{CC} (min)	HT	HL	HH	HV	Z	HV
Hold Cycle	≥ V_{CC} (min)	HV or HT	HL	HL	X	X	X
Single Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	HT	HL	HH	X	Z	HV
Single Latency (Dummy) Cycle	≥ V_{CC} (min)	HT	HL	HH	X	Z	X
Single Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	HT	HL	HH	X	MV	X
Dual Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	HT	HL	HH	X	HV	HV
Dual Latency (Dummy) Cycle	≥ V_{CC} (min)	HT	HL	HH	X	X	X
Dual Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	HT	HL	HH	X	MV	MV
Quad Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	HT	HL	HV	HV	HV	HV
Quad Latency (Dummy) Cycle	≥ V_{CC} (min)	HT	HL	X	X	X	X
Quad Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	HT	HL	MV	MV	MV	MV

Legend:
Z = no driver - floating signal
HL = Host driving V_{IL}
HH = Host driving V_{IH}
HV = either HL or HH
X = HL or HH or Z
HT = toggling between HL and HH
ML = Memory driving V_{IL}
MH = Memory driving V_{IH}
MV = either ML or MH

4.3.1 Low Power Hardware Data Protection

When V_{CC} is less than V_{WI} the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

4.3.2 Power-On (Cold) Reset

When the core voltage supply remains at or below the V_{WI} voltage for ≥ t_{PD} time, then rises to ≥ $V_{CC\ (Minimum)}$ the device will begin its Power-On-Reset (POR) process. POR continues until the end of t_{PUW}. During t_{PUW} the device does not react to write commands. Following the end of t_{PUW} the device transitions to the Interface Standby state and can accept write commands. For additional information on POR see *Power On (Cold) Reset* on page 30.

4.3.3 Interface Standby

When CS# is high the SPI interface is in standby state. Inputs are ignored. The interface waits for the beginning of a new command. The next interface state is Instruction Cycle when CS# goes low to begin a new command.

While in interface standby state the memory device draws standby current (I_{SB}) if no embedded algorithm is in progress. If an embedded algorithm is in progress, the related current is drawn until the end of the algorithm when the entire device returns to standby current draw.

4.3.4 Instruction Cycle

When the host drives the MSB of an instruction and CS# goes low, on the next rising edge of SCK the device captures the MSB of the instruction that begins the new command. On each following rising edge of SCK the device captures the next lower significance bit of the 8-bit instruction. The host keeps CS# low, HOLD# high, and drives Write Protect (WP#) signal as needed for the instruction. However, WP# is only relevant during instruction cycles of a Write Status Registers command and is otherwise ignored.

Each instruction selects the address space that is operated on and the transfer format used during the remainder of the command. The transfer format may be Single, Dual output, Quad output, Dual I/O, or Quad I/O. The expected next interface state depends on the instruction received.

Some commands are stand alone, needing no address or data transfer to or from the memory. The host returns CS# high after the rising edge of SCK for the eighth bit of the instruction in such commands. The next interface state in this case is Interface Standby.

4.3.5 Hold

When Quad mode is not enabled (SR2[1]=0) the HOLD# / IO3 signal is used as the HOLD# input. The host keeps HOLD# low, SCLK may be at a valid level or continue toggling, and CS# is low. When HOLD# is low a command is paused, as though SCK were held low. SI / IO0 and SO / IO1 ignore the input level when acting as inputs and are high impedance when acting as outputs during hold state. Whether these signals are input or output depends on the command and the point in the command sequence when HOLD# is asserted low.

When HOLD# returns high the next state is the same state the interface was in just before HOLD# was asserted low.

4.3.6 Single Input Cycle - Host to Memory Transfer

Several commands transfer information after the instruction on the single serial input (SI) signal from host to the memory device. The dual output, and quad output commands send address to the memory using only SI but return read data using the I/O signals. The host keeps CS# low, HOLD# high, and drives SI as needed for the command. The memory does not drive the Serial Output (SO) signal.

The expected next interface state depends on the instruction. Some instructions continue sending address or data to the memory using additional Single Input Cycles. Others may transition to Single Latency, or directly to Single, Dual, or Quad Output.

4.3.7 Single Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the instruction. During the latency cycles, the host keeps CS# low, and HOLD# high. The Write Protect (WP#) signal is ignored. The host may drive the SI signal during these cycles or the host may leave SI floating. The memory does not use any data driven on SI / I/O0 or other I/O signals during the latency cycles. In dual or quad read commands, the host must stop driving the I/O signals on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving I/O signals during latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the Serial Output (SO) or I/O signals during the latency cycles.

The next interface state depends on the command structure i.e. the number of latency cycles, and whether the read is single, dual, or quad width.

4.3.8 Single Output Cycle - Memory to Host Transfer

Several commands transfer information back to the host on the single Serial Output (SO) signal. The host keeps CS# low, and HOLD# high. The Write Protect (WP#) signal is ignored. The memory ignores the Serial Input (SI) signal. The memory drives SO with data.

The next interface state continues to be Single Output Cycle until the host returns CS# to high ending the command.

4.3.9 Dual Input Cycle - Host to Memory Transfer

The Read Dual I/O command transfers two address or mode bits to the memory in each cycle. The host keeps CS# low, HOLD# high. The Write Protect (WP#) signal is ignored. The host drives address on SI / IO0 and SO / IO1.

The next interface state following the delivery of address and mode bits is a Dual Latency Cycle if there are latency cycles needed or Dual Output Cycle if no latency is required.

4.3.10 Dual Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the instruction. During the latency cycles, the host keeps CS# low, and HOLD# high. The Write Protect (WP#) signal is ignored. The host may drive the SI / IO0 and SO / IO1 signals during these cycles or the host may leave SI / IO0 and SO / IO1 floating. The memory does not use any data driven on SI / IO0 and SO / IO1 during the latency cycles. The host must stop driving SI / IO0 and SO / IO1 on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the SI / IO0 and SO / IO1 signals during the latency cycles.

The next interface state following the last latency cycle is a Dual Output Cycle.

4.3.11 Dual Output Cycle - Memory to Host Transfer

The Read Dual Output and Read Dual I/O return data to the host two bits in each cycle. The host keeps CS# low, and HOLD# high. The Write Protect (WP#) signal is ignored. The memory drives data on the SI / IO0 and SO / IO1 signals during the dual output cycles.

The next interface state continues to be Dual Output Cycle until the host returns CS# to high ending the command.

4.3.12 Quad Input Cycle - Host to Memory Transfer

The Read Quad I/O command transfers four address, mode, or data bits to the memory in each cycle. The host keeps CS# low, and drives the IO signals.

For Read Quad I/O the next interface state following the delivery of address and mode bits is a Quad Latency Cycle if there are latency cycles needed or Quad Output Cycle if no latency is required.

4.3.13 Quad Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Control in the Status Register-3 (SR3[3:0]). During the latency cycles, the host keeps CS# low. The host may drive the IO signals during these cycles or the host may leave the IO floating. The memory does not use any data driven on IO during the latency cycles. The host must stop driving the IO signals on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the IO signals during the latency cycles.

The next interface state following the last latency cycle is a Quad Output Cycle.

4.3.14 Quad Output Cycle - Memory to Host Transfer

The Read Quad Output and Read Quad I/O return data to the host four bits in each cycle. The host keeps CS# low. The memory drives data on IO0-IO3 signals during the Quad output cycles.

The next interface state continues to be Quad Output Cycle until the host returns CS# to high ending the command.

4.4 Status Register Effects on the Interface

The Status Register-2, bit 1 (SR2[1]), selects whether Quad mode is enabled to ignore HOLD# and WP# and allow Read Quad Output, and Read Quad I/O commands.

4.5 Data Protection

Some basic protection against unintended changes to stored data are provided and controlled purely by the hardware design. These are described below. Other software managed protection methods are discussed in the software section of this document.

4.5.1 Low Power

When V_{CC} is less than V_{WI} the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

4.5.2 Power-Up

Program and erase operations continue to be prevented during the Power-up to Write delay (t_{PUW}) because no write command is accepted until after t_{PUW}.

4.5.3 Deep-Power-Down (DPD)

In DPD mode the device responds only to the Resume from DPD command (RES ABh). All other commands are ignored during DPD mode, thereby protecting the memory from program and erase operations.

4.5.4 Clock Pulse Count

The device verifies that all program, erase, and Write Status Registers commands consist of a clock pulse count that is a multiple of eight before executing them. A command not having a multiple of 8 clock pulse count is ignored and no error status is set for the command.

5. Electrical Characteristics

Specifications for the S25FL116K are Advance Information and subject to change.

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Parameters(1)	Symbol	Conditions	Range	Unit
Supply Voltage	V_{CC}		–0.6 to +4.0	V
Voltage Applied to Any Pin	V_{IO}	Relative to Ground	–0.6 to +4.0	V
Transient Voltage on any Pin	V_{IOT}	< 20 ns Transient Relative to Ground	–2.0 to 6.0	V
Storage Temperature	T_{STG}		–65 to +150	°C
Lead Temperature	T_{LEAD}		(2)	°C
Electrostatic Discharge Voltage	V_{ESD}	Human Body Model (3)	–2000 to +2000	V

Notes:

1. *This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.*
2. *Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.*
3. *JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 ohms, R2=500 ohms).*

5.1.1 Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{CC}. During voltage transitions, inputs or I/Os may overshoot V_{SS} to negative V_{IOT} or overshoot to positive V_{IOT}, for periods up to 20 ns.

Figure 5.1 Maximum Negative Overshoot Waveform

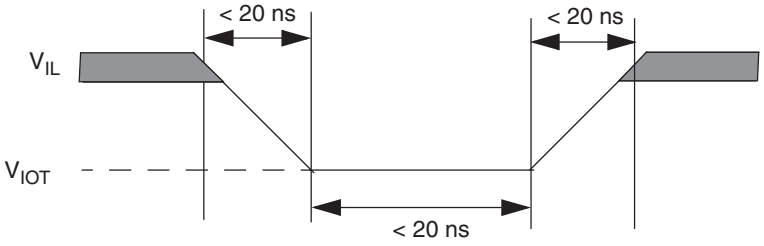
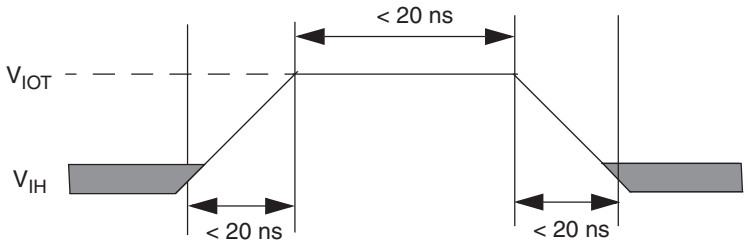


Figure 5.2 Maximum Positive Overshoot Waveform



5.1.2 Latchup Characteristics

Table 5.2 Latchup Specification

Description	Min	Max	Unit
Input voltage with respect to V_{SS} on all input only connections	–1.0	V_{CC} + 1.0	V
Input voltage with respect to V_{SS} on all I/O connections	–1.0	V_{CC} + 1.0	V
V_{CC} Current	–100	+100	mA

Note:
1. *Excludes power supply V_{CC}. Test conditions: V_{CC} = 3.0 V, one connection at a time tested, connections not being tested are at V_{SS}.*

5.2 Operating Ranges

Operating ranges define those limits between which functionality of the device is guaranteed.

Table 5.3 Operating Ranges

Parameter	Symbol	Conditions	Spec		Unit
			Min	Max	
Ambient Temperature	T_A	Industrial	–40	+85	°C
Supply Voltage	V_{CC}	Full Range	2.7	3.6	V

Note:
1. *V_{CC} voltage during read can operate across the min and max range but should not exceed ± 10% of the voltage used during programming or erase of the data being read.*

5.3 DC Electrical Characteristics

Table 5.4 DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN} (1)	V_{IN} = 0V (1)			6	pF
Output Capacitance	C_{OUT} (1)	V_{OUT} = 0V (1)			8	pF
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	I_{CC1}	CS# = V_{CC}, V_{IN} = GND or V_{CC}		15	25	µA
Power-down Current	I_{CC2}	CS# = V_{CC}, V_{IN} = GND or V_{CC}		2	5	µA
Current: Read Single/Dual/Quad 1 MHz (2)	I_{CC3}	SCK = 0.1 V_{CC} / 0.9 V_{CC} SO = Open		4/5/6	6/7.5/9	mA
Current: Read Single/Dual/Quad 33 MHz (2)	I_{CC3}	SCK = 0.1 V_{CC} / 0.9 V_{CC} SO = Open		6/7/8	9/10.5/12	mA
Current: Read Single/Dual/Quad 50 MHz (2)	I_{CC3}	SCK = 0.1 V_{CC} / 0.9 V_{CC} SO = Open		7/8/9	10/12/13.5	mA
Current: Read Single/Dual/Quad 108 MHz (2)	I_{CC3}	SCK = 0.1 V_{CC} / 0.9 V_{CC} SO = Open		12/14/16	18/22/25	mA
Current: Write Status Registers	I_{CC4}	CS# = V_{CC}		8	12	mA
Current Page Program	I_{CC5}	CS# = V_{CC}		20	25	mA
Current Sector/Block Erase	I_{CC6}	CS# = V_{CC}		20	25	mA
Current Chip Erase	I_{CC7}	CS# = V_{CC}		20	25	mA
Input Low Voltage	V_{IL}		-0.5		V_{CC} x 0.2	V
Input High Voltage	V_{IH}		V_{CC} x 0.7		V_{CC} + 0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 100 µA	V_{SS}		0.2	V
		I_{OL} = 1.6 mA	V_{SS}		0.4	
Output High Voltage	V_{OH}	I_{OH} = –100 µA	V_{CC} – 0.2		V_{CC}	V

Notes:
1. *Tested on sample basis and specified through design and characterization data. T_A = 25°C, V_{CC} = 3V.*
2. *Checker Board Pattern.*

5.3.1 Active Power and Standby Power Modes

The device is enabled and in the Active Power mode when Chip Select (CS#) is Low. When CS# is high, the device is disabled, but may still be in an Active Power mode until all program, erase, and write operations have completed. The device then goes into the Standby Power mode, and power consumption drops to I_{SB}.

5.4 AC Measurement Conditions

Figure 5.3 Test Setup

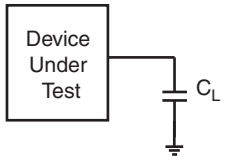


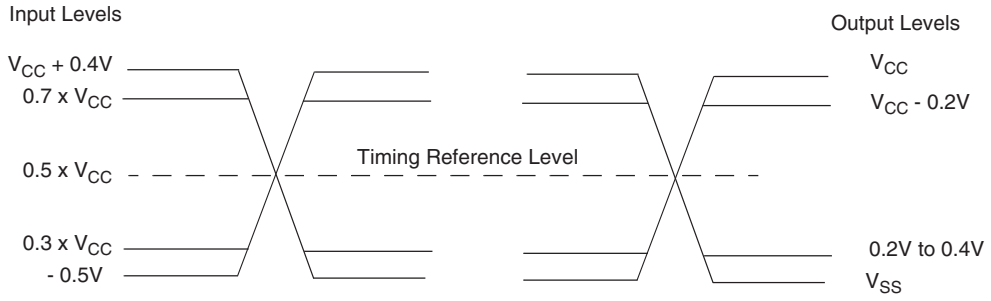
Table 5.5 AC Measurement Conditions

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance		30	pF
TR, TF	Input Rise and Fall Times		2.4	ns
	Input Pulse Voltage	0.2 x V_{CC} to 0.8 V_{CC}		V
	Input Timing Ref Voltage	0.5 V_{CC}		V
	Output Timing Ref Voltage	0.5 V_{CC}		V

Notes:

1. *Output High-Z is defined as the point where data is no longer driven.*
2. *Input slew rate: 1.5 V/ns.*
3. *AC characteristics tables assume clock and data signals have the same slew rate (slope).*

Figure 5.4 Input, Output, and Timing Reference Levels



5.4.1 Capacitance Characteristics

Table 5.6 Capacitance

	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance (applies to SCK, CS#)	1 MHz		8	pF
C_{OUT}	Output Capacitance (applies to All I/O)	1 MHz		8	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

5.5 Power-up Timing

Table 5.7 Power-Up Timing and Voltage Levels

Parameter	Symbol	Spec		Unit
		Min	Max	
V_{CC} (min) to CS# Low	t_{VSL}	10		µs
Time Delay Before Write Command	t_{PUW}	1	10	ms
Write Inhibit Threshold Voltage	V_{WI}	1.0	2.0	V

Note:
1. These parameters are characterized only.

Figure 5.5 Power-Up Timing and Voltage Levels

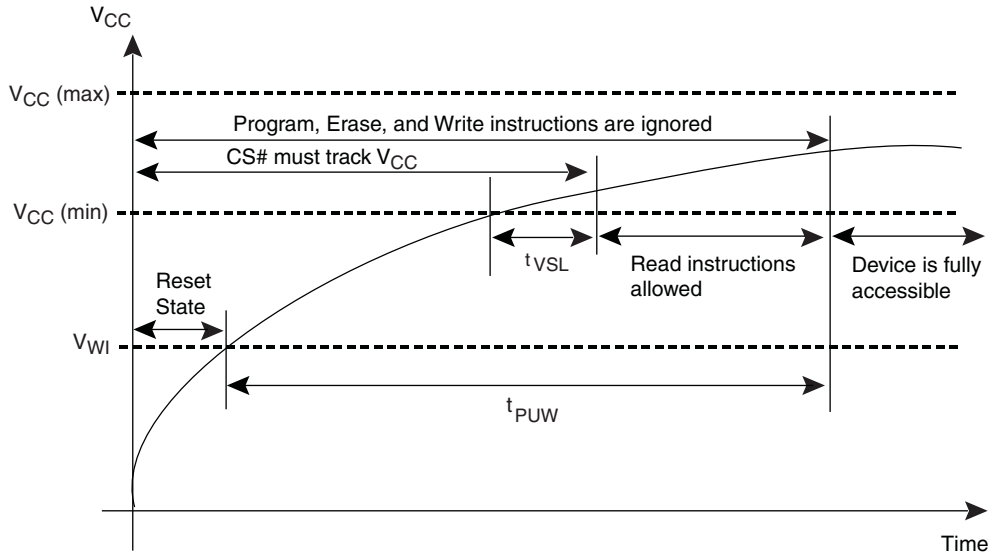
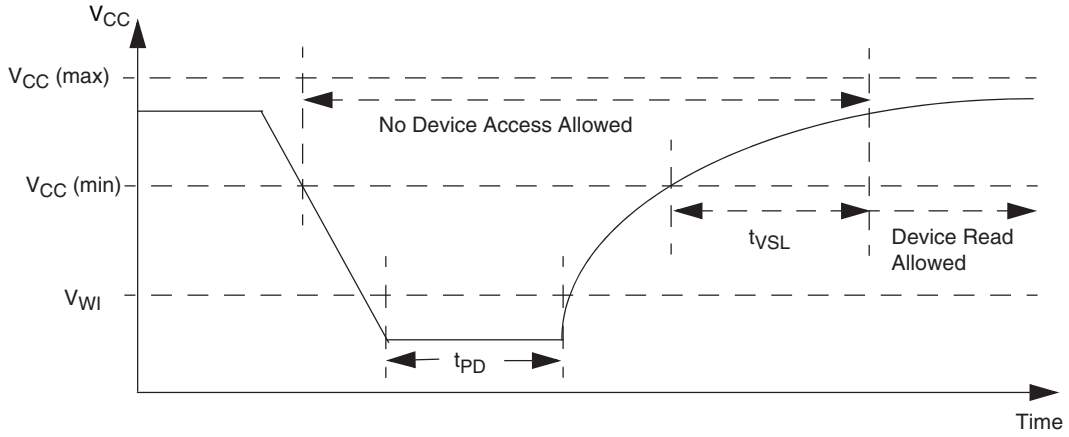


Figure 5.6 Power-Down and Voltage Drop



5.6 Power On (Cold) Reset

The device executes a Power-On-Reset (POR) process until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold. See Figure 5.5 on page 29, Figure 5.6 on page 29, and Table on page 29. The device must not be selected (CS# to go high with V_{CC}) until after (t_{VSL}), i.e. no commands may be sent to the device until the end of t_{VSL}.

5.7 AC Electrical Characteristics

Table 5.8 Industrial Temperature Ranges (Sheet 1 of 2)

Description	Symbol	Alt	Spec			Unit
			Min	Typ	Max	
Clock frequency for all SPI commands except for Read Data command (03h) and Fast Read command (0Bh) 2.7V-3.6V V_{CC}	F_R	f_C	D.C.		108	MHz
Clock frequency for Read Data command (03h)	f_R		D.C.		50	MHz
Clock frequency for all Fast Read commands SIO and MIO	f_{FR}		D.C.		108	MHz
Clock Period	P_{SCK}		9.25			ns
Clock High, Low Time for f_{FR}	t_{CLH}, t_{CLL} (1)	t_{CH}, t_{CL}	3.3			ns
Clock High, Low Time for F_R	t_{CLH}, t_{CLL} (1)	t_{CH}, t_{CL}	4.3			ns
Clock High, Low Time for f_R	t_{CRLH}, t_{CRLL} (1)	t_{CH}, t_{CL}	6			ns
Clock Rise Time	t_{CLCH} (2)	t_{CRT},	0.1			V/ns
Clock Fall Time	t_{CHCL} (2)	t_{CFT}	0.1			V/ns
CS# Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	5			ns
CS# Not Active Hold Time relative to CLK	t_{CHSL}	t_{CSH}	5			ns
Data In Setup Time	t_{DVCH}	t_{SU}	2			ns
Data In Hold Time	t_{CHDX}	t_{HD}	5			ns
CS# Active Hold Time relative to CLK	t_{CHSH}	t_{CSS}	5			ns
CS# Not Active Setup Time relative to CLK	t_{SHCH}	t_{CSH}	5			ns
CS# Deselect Time (for Array Read -> Array Read)	t_{SHSL1}	t_{CS1}	7			ns
CS# Deselect Time (for Erase or Program -> Read Status Registers) Volatile Status Register Write Time	t_{SHSL2}	t_{CS2}	40 40			ns
Output Disable Time	t_{SHQZ} (2)	t_{DIS}			7	ns
Clock Low to Output Valid, 30 pF, 2.7V - 3.6V	t_{CLQV1}	t_{V1}			7	ns
Clock Low to Output Valid, 15 pF, 2.7V - 3.6V	t_{CLQV1}	t_{V1}			6	ns
Clock Low to Output Valid (for Read ID commands) 2.7V - 3.6V	t_{CLQV2}	t_{V2}			8.5	ns
Output Hold Time	t_{CLQX}	t_{HO}	2			ns
HOLD# Active Setup Time relative to CLK	t_{HLCH}		5			ns
HOLD# Active Hold Time relative to CLK	t_{CHHH}		5			ns
HOLD# Not Active Setup Time relative to CLK	t_{HHCH}		5			ns
HOLD# Not Active Hold Time relative to CLK	t_{CHHL}		5			ns
HOLD# to Output Low-Z	t_{HHQX} (2)	t_{LZ}			7	ns
HOLD# to Output High-Z	t_{HLQZ} (2)	t_{HZ}			12	ns
Write Protect Setup Time Before CS# Low	t_{WHSL} (3)	t_{WPS}	20			ns
Write Protect Hold Time After CS# High	t_{SHWL} (3)	t_{WPH}	100			ns
CS# High to Power-down Mode	t_{DP} (2)				3	µs
CS# High to Standby Mode without Electronic Signature Read	t_{RES1} (2)				3	µs
CS# High to Standby Mode with Electronic Signature Read	t_{RES2} (2)				1.8	µs
Write Status Registers Time	t_W			50	300	ms

Table 5.8 Industrial Temperature Ranges (Sheet 2 of 2)

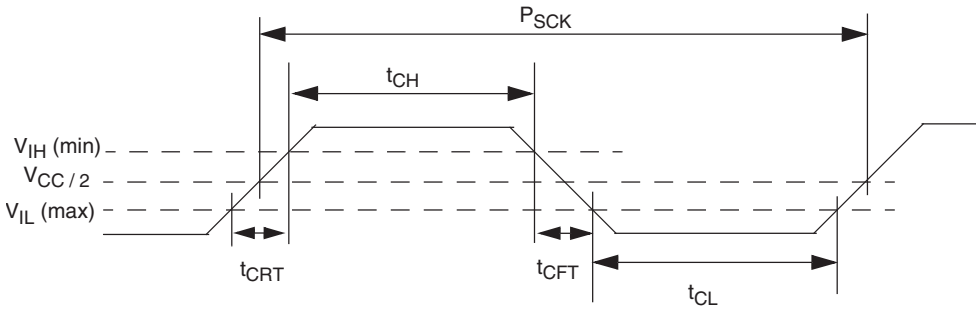
Description	Symbol	Alt	Spec			Unit
			Min	Typ	Max	
Byte Program Time (First Byte) (4)(5)	t_{BP1}			15	50	µs
Additional Byte Program Time (After First Byte) (4)(5)	t_{BP2}			2.5	12	µs
Page Program Time (5)	t_{PP}			0.7	3	ms
Sector Erase Time (4 kB) (5)	t_{SE}			70	450	ms
Block Erase Time (64 kB) (5)	t_{BE2}			500	2000	ms
Chip Erase Time 16 Mb (5)	t_{CE}			11.2	64	s

Notes:

1. *Clock high + Clock low must be less than or equal to $1/f_C$.*
2. *Value guaranteed by design and/or characterization, not 100% tested in production.*
3. *Only applicable as a constraint for a Write Status Registers command when Status Register Protect 0 (SRP0) bit is set to 1. Or WPSEL bit = 1.*
4. *For multiple bytes after first byte within a page, $t_{BPN} = t_{BP1} + t_{BP2} * N$ (typical) and $t_{BPN} = t_{BP1} + t_{BP2} * N$ (max), where N = number of bytes programmed.*
5. *All program and erase times are tested using a random data pattern.*

5.7.1 Clock Timing

Figure 5.7 Clock Timing



5.7.2 Input / Output Timing

Figure 5.8 SPI Single Bit Input Timing

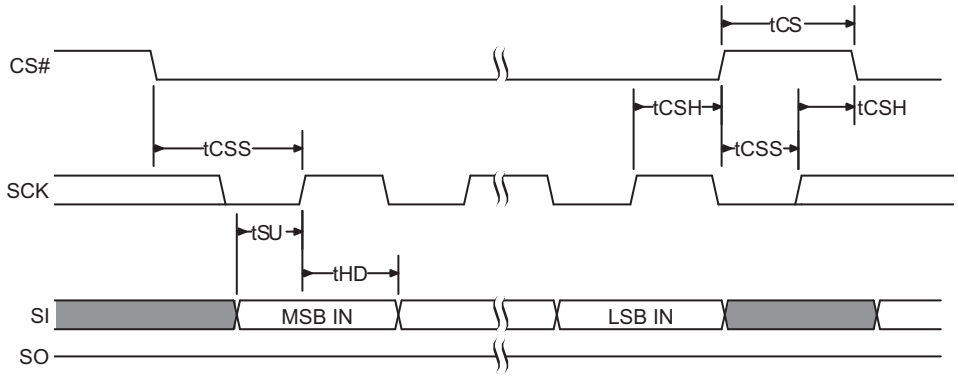


Figure 5.9 SPI Single Bit Output Timing

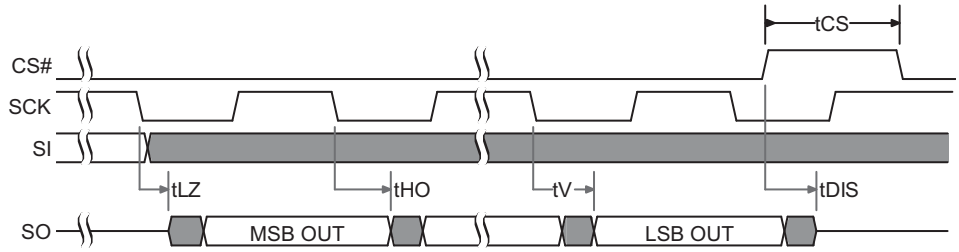


Figure 5.10 SPI MIO Timing

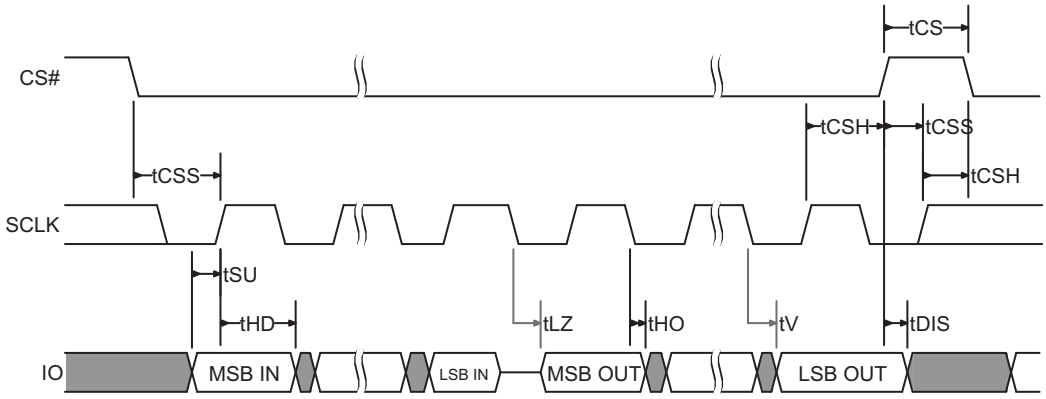


Figure 5.11 Hold Timing

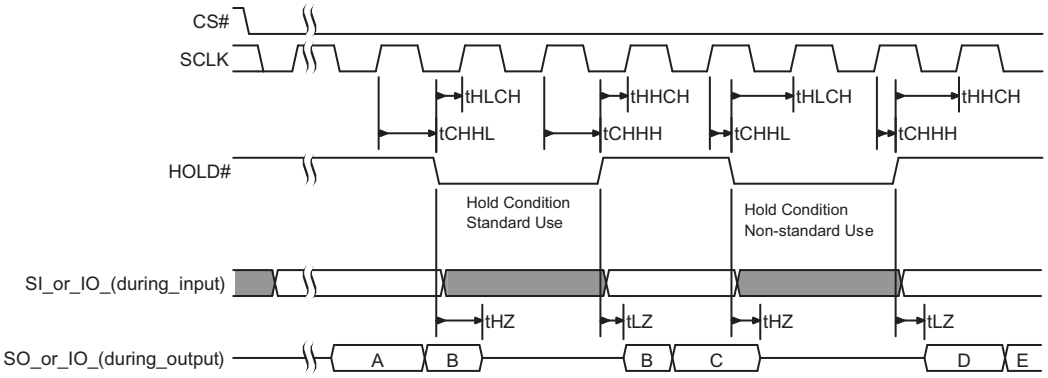
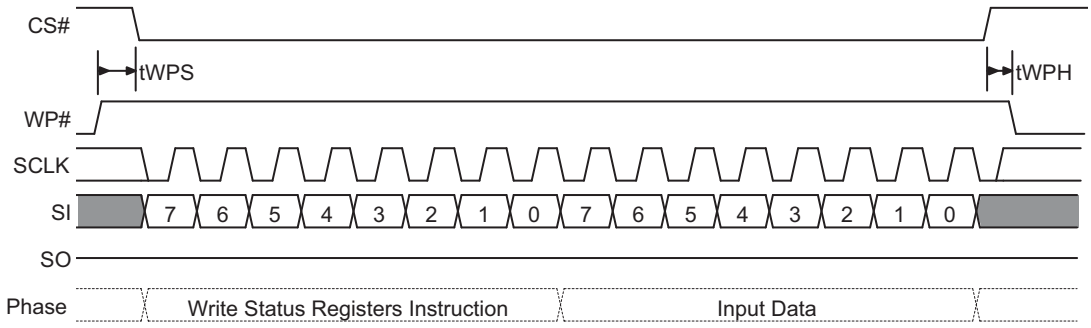


Figure 5.12 WP# Input Timing



6. Physical Interface

6.1 Connection Diagrams

6.1.1 SOIC 8 / USON 8

Table 6.1 8-Connector Package, Top View

Signal	Lead	Package Body	Lead	Signal
CS#	1	SOIC 8 USON 8	8	VCC
SO / IO1	2		7	HOLD# / IO3
WP# / IO2	3		6	SCLK
VSS	4		5	SI / IO0

6.1.2 FAB024 24-Ball BGA

Table 6.2 24-Ball BGA, 5x5 Ball Footprint (FAB024), Top View

Ball Index	1	2	3	4	5
A	(no ball)	NC	NC	RFU	NC
B	DNU	SCLK	VSS	VCC	NC
C	DNU	CS#	RFU	WP# / IO2	NC
D	DNU	SO / IO1	SI / IO0	HOLD# / IO3	NC
E	NC	NC	NC	RFU	NC

6.1.3 FAC024 24-Ball BGA Package

Table 6.3 24-Ball BGA, 4x6 Ball Footprint (FAC024), Top View

Ball Index	1	2	3	4
A	NC	NC	NC	RFU
B	DNU	SCK	VSS	VCC
C	DNU	CS#	RFU	WP# / IO2
D	DNU	SO / IO1	SI / IO0	HOLD# / IO3
E	NC	NC	NC	RFU
F	NC	NC	NC	NC

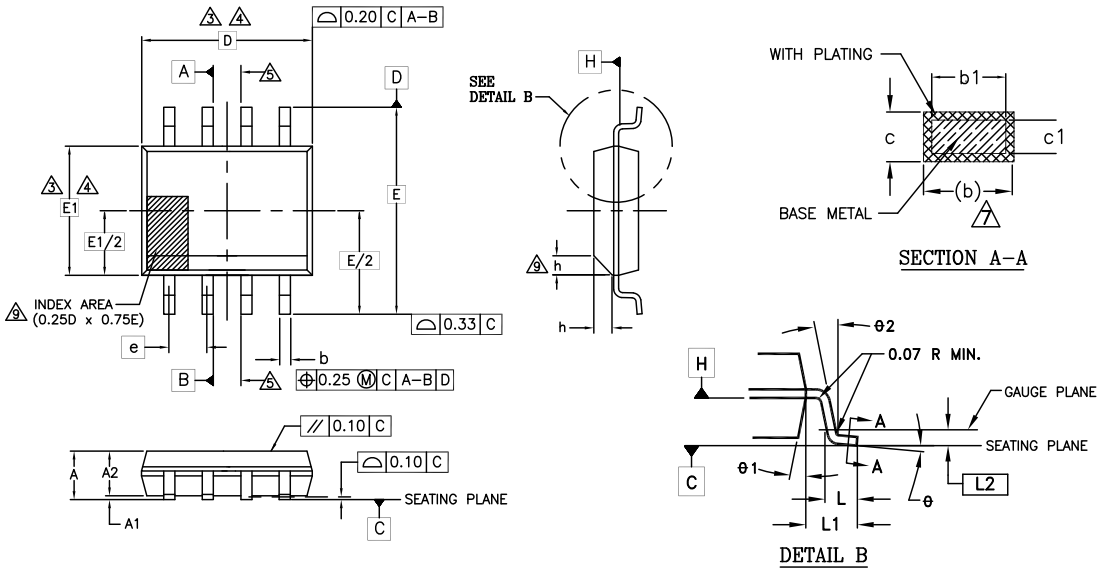
Note:
1. Signal connections are in the same relative positions as FAB024 BGA, allowing a single PCB footprint to use either package.

6.1.4 Special Handling Instructions for FBGA Packages

Flash memory devices in BGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

6.2 Physical Diagrams

6.2.1 SOA008 — 8-lead Plastic Small Outline Package (150-mils Body Width)



PACKAGE	SOA 008(INCHES)		SOA 008(MM)	
JEDEC	MS-012(D)AA		MS-012(D)AA	
SYMBOL	MIN	MAX	MIN	MAX
A	0.0531	0.0688	1.35	1.75
A1	0.0039	0.0098	0.10	0.25
A2	0.052	0.061	1.32	1.55
b	0.012	0.020	0.31	0.51
b1	0.011	0.019	0.27	0.48
c	0.0067	0.0098	0.17	0.25
c1	0.0067	0.009	0.17	0.23
D	0.193 BSC		4.90 BSC	
E	0.236 BSC		6.00 BSC	
E1	0.1535 BSC		3.90 BSC	
e	0.050 BSC		1.27 BSC	
L	0.0161	0.035	0.41	0.89
L1	0.041 REF		1.04 REF	
L2	0.010 BSC		0.25 BSC	
N	8		8	
h	0.10	0.196	0.25	0.50
θ	0°	8°	0°	8°
θ1	5°	15°	5°	15°
θ2	0° REF		0° REF	

NOTES:

1. ALL DIMENSIONS ARE IN BOTH INCHES AND MILLMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH. BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

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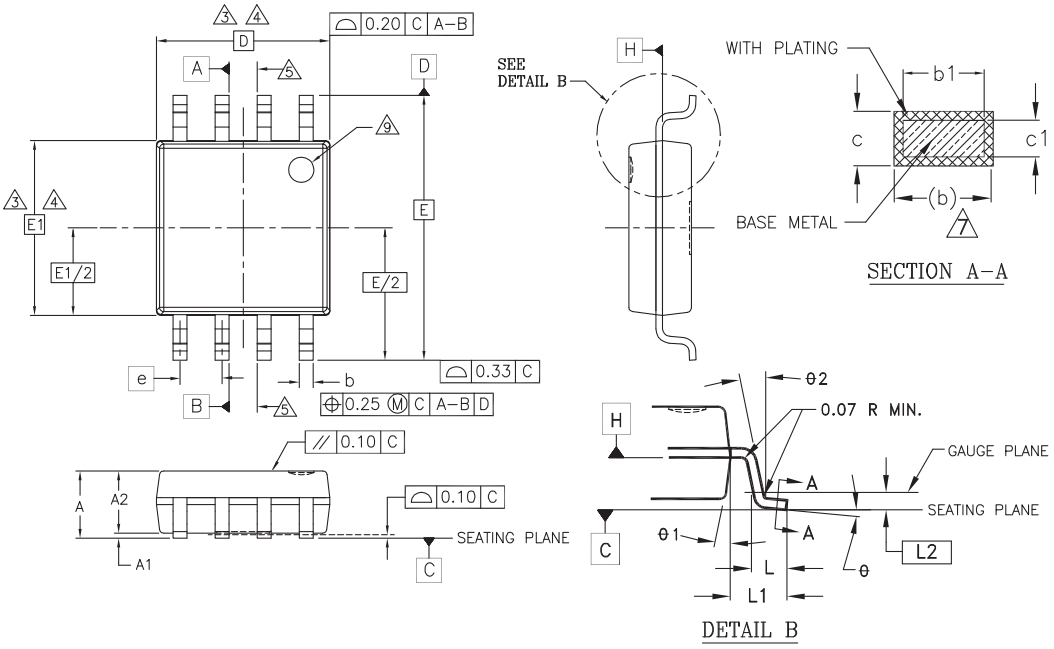
6.2.2 SOC008 — 8-lead Plastic Small Outline Package (208-mils Body Width)



PACKAGE	SOC 008 (inches)		SOC 008 (mm)	
JEDEC				
SYMBOL	MIN	MAX	MIN	MAX
A	0.069	0.085	1.753	2.159
A1	0.002	0.0098	0.051	0.249
A2	0.067	0.075	1.70	1.91
b	0.014	0.019	0.356	0.483
b1	0.013	0.018	0.330	0.457
c	0.0075	0.0095	0.191	0.241
c1	0.006	0.008	0.152	0.203
D	0.208 BSC		5.283 BSC	
E	0.315 BSC		8.001 BSC	
E1	0.208 BSC		5.283 BSC	
e	.050 BSC		1.27 BSC	
L	0.020	0.030	0.508	0.762
L1	.049 REF		1.25 REF	
L2	.010 BSC		0.25 BSC	
N	8		8	
θ	0°	8°	0°	8°
θ1	5°	15°	5°	15°
θ2	0°		0°	

NOTES:

1. ALL DIMENSIONS ARE IN BOTH INCHES AND MILLMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH. BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

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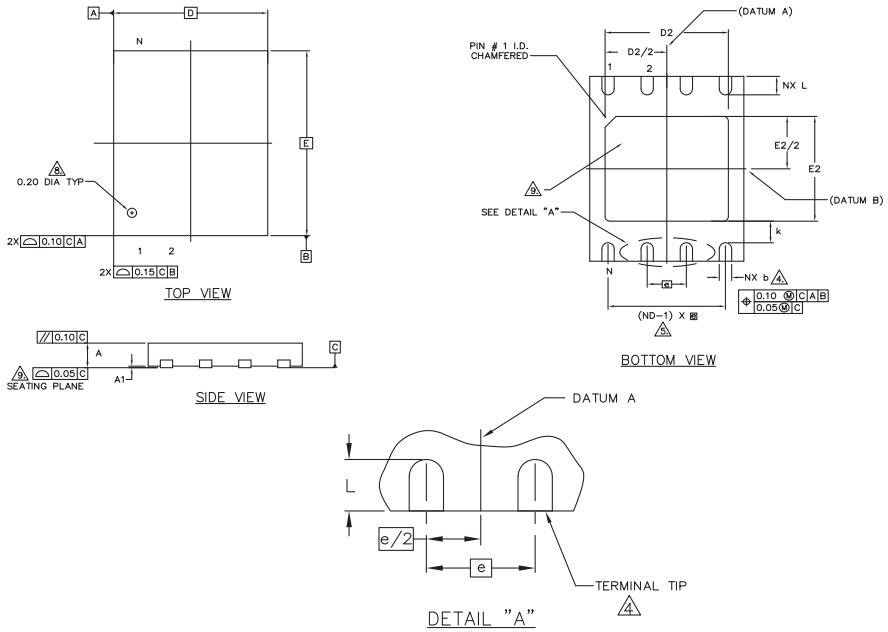
6.2.3 WND008 — 8-contact USON 5x6



PACKAGE	WND008			
SYMBOL	MIN	NOM	MAX	NOTES
e		1.27 BSC.		
N		8		3
ND		4		5
L	0.55	0.60	0.65	
b	0.35	0.40	0.45	4
D2	3.90	4.00	4.10	
E2	3.30	3.40	3.50	
D		5.00 BSC		
E		6.00 BSC		
A	0.70	0.75	0.80	
A1	0.00	0.02	0.05	
K		0.20 MIN.		

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M - 1994.
2. ALL DIMENSIONS ARE IN MILLMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION “b” APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION “b” SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

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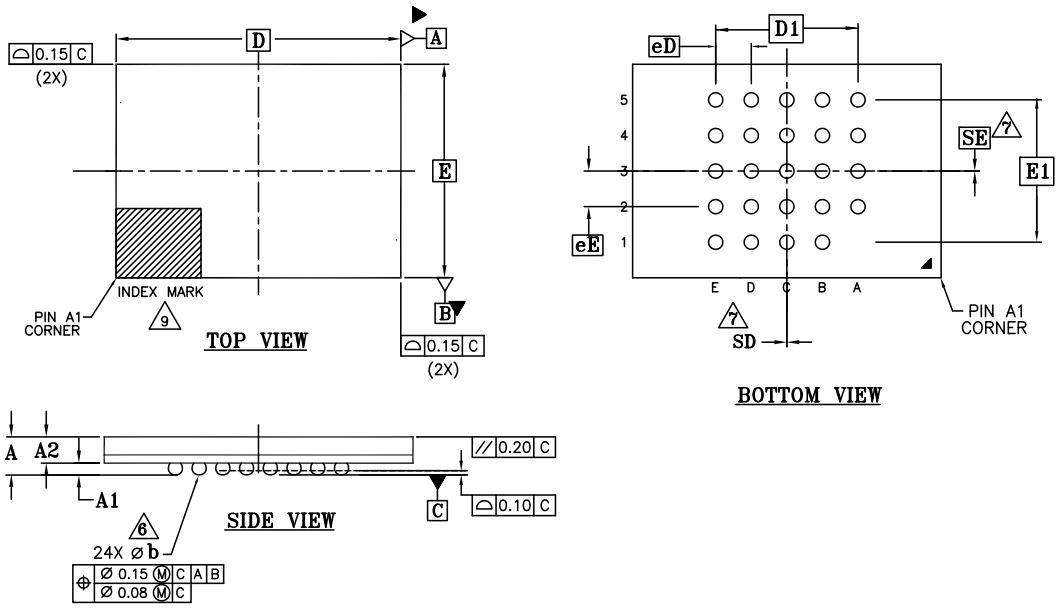
6.2.4 FAB024 — 24-ball Ball Grid Array (8 x 6 mm) Package



PACKAGE	FAB024			
JEDEC	N/A			
	8.00mmx6.00mm NOM PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	NOTE
A	–	–	1.20	OVERALL THICKNESS
A1	0.20	–	–	BALL HEIGHT
A2	0.70	–	0.90	BODY THICKNESS
D	8.00 BSC.			BODY SIZE
E	6.00 BSC.			BODY SIZE
D1	4.00 BSC.			BALL FOOTPRINT
E1	4.00 BSC.			BALL FOOTPRINT
MD	5			ROW MATRIX SIZE D DIRECTION
ME	5			ROW MATRIX SIZE E DIRECTION
N	24			TOTAL BALL COUNT
øb	0.35	0.40	0.45	BALL DIAMETER
e	1.00 BSC.			BALL PITCH
SD/SE	0.00			SOLDER BALL PLACEMENT
	A1			DEPOPULATED SOLDER BALLS
	I			PACKAGE OUTLINE TYPE

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP–010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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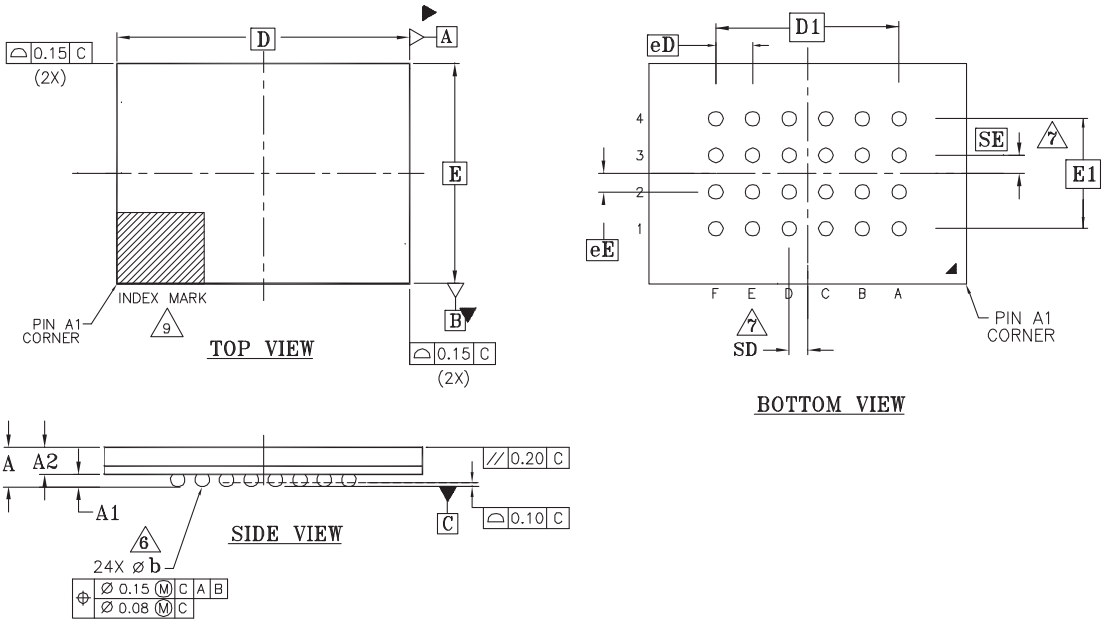
6.2.5 FAC024 — 24-ball Ball Grid Array (8 x 6 mm) Package



PACKAGE	FAC024			
JEDEC	N/A			
D x E	8.00 mm x 6.00 mm NOM PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.25	---	---	BALL HEIGHT
A2	0.70	---	0.90	BODY THICKNESS
D	8.00 BSC.			BODY SIZE
E	6.00 BSC.			BODY SIZE
D1	5.00 BSC.			MATRIX FOOTPRINT
E1	3.00 BSC.			MATRIX FOOTPRINT
MD	6			MATRIX SIZE D DIRECTION
ME	4			MATRIX SIZE E DIRECTION
N	24			BALL COUNT
Øb	0.35	0.40	0.45	BALL DIAMETER
e	1.00 BSC.			BALL PITCHL
SD/ SE	0.5/0.5			SOLDER BALL PLACEMENT
				DEPOPULATED SOLDER BALLS
	J			PACKAGE OUTLINE TYPE

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

   DATUM C IS THE SEATING PLANE AND IS DEFINED BY THE CROWNS OF THE SOLDER BALLS.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

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Software Interface

This section discusses the features and behaviors most relevant to host system software that interacts with S25FL116K memory devices.

7. Address Space Maps

7.1 Overview

Many commands operate on the main flash memory array. Some commands operate on address spaces separate from the main flash array. Each separate address space uses the full 24-bit address but may only define a small portion of the available address space.

7.2 Flash Memory Array

The main flash array is divided into erase units called sectors. The sectors are uniform 4 kbytes in size.

Table 7.1 S25FL116K Main Memory Address Map

Sector Size (kbyte)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
4	512	SA0	000000h-000FFFh	Sector Starting Address
		:	:	—
		SA511	1FF000h-1FFFFFh	Sector Ending Address

Note:
This is condensed table that use a couple of sectors as references. There are address ranges that are not explicitly listed. All 4-kB sectors have the pattern XXX000h-XXXFFFh.

7.3 Security Registers

The S25FL116K provides four 256-byte Security Registers. Each register can be used to store information that can be permanently protected by programming One Time Programmable (OTP) lock bits in Status Register-2.

Register 0 is used by Spansion to store and protect the Serial Flash Discoverable Parameters (SFDP) information that is also accessed by the Read SFDP command.

The three additional Security Registers can be erased, programmed, and protected individually. These registers may be used by system manufacturers to store and permanently protect security or other important information separate from the main memory array.

Table 7.2 Security Register Addresses

Security Register	Address
0 (SFDP)	000000h - 0000FF
1	001000h - 0010FF
2	002000h - 0020FF
3	003000h - 0030FF

7.3.1 Security Register 0 - Serial Flash Discoverable Parameters (SFDP)

The S25FL116K features a 256-Byte Serial Flash Discoverable Parameter (SFDP) space, located in Security Register 0, that contains information about the device operational capabilities such as available commands, timing and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified but more may be added in the future. The Read SFDP Register command reads the contents of Security Register 0 and is compatible with the JEDEC JESD216 SFDP standard.

Table 7.3 Serial Flash Discoverable Parameter Definition Table (Sheet 1 of 2)

DWORD	Byte Address	Data	Description	Comment
SFDP Header 1	00h	53h	SFDP Signature	SFDP Signature = 50444653h
	01h	46h	SFDP Signature	
	02h	44h	SFDP Signature	
	03h	50h	SFDP Signature	
SFDP Header 2	04h	00h	SFDP Minor Revisions	SFDP revision 1.0
	05h	01h	SFDP Major Revisions	
	06h	02h	Number of Parameter Headers (NPH)	3 Parameter Headers
	07h	FFh	Reserved	
Parameter Header 1	08h	00h	PID(0): Parameter ID (1)	Mandatory JEDEC Parameter = 00h
	09h	00h	PID(0): JEDEC Parameter Minor Revisions	JEDEC Parameter Version 1.0 as published in JESD216 April 2011
	0Ah	01h	PID(0): JEDEC Parameter Major Revisions	
	0Bh	09h	PID(0): JEDEC Parameter Length	9 Dwords
Parameter Header 2	0Ch	80h	PID(0): Address of Parameter Table (A7-A0)	PID(0) Table Address = 000080h
	0Dh	00h	PID(0): Address of Parameter Table (A15-A8)	
	0Eh	00h	PID(0): Address of Parameter Table (A23-A16)	
	0Fh	FFh	Reserved	
Parameter Header 3	10h	EFh	PID(1): Parameter ID	Legacy Parameter ID = EFh
	11h	00h	PID(1): Parameter Minor Revisions	Serial Flash Basics Version 1.0
	12h	01h	PID(1): Parameter Major Revisions	
	13h	04h	PID(1): Parameter Length	4 Dwords
Parameter Header 4	14h	A4h	PID(1): Address of Parameter Table (A7-A0)	PID(1) Table Address = 000080h Same data as first 4 words of JEDEC Parameter
	15h	00h	PID(1): Address of Parameter Table (A15-A8)	
	16h	00h	PID(1): Address of Parameter Table (A23-A16)	
	17h	FFh	Reserved	
Parameter Header 5	18h	01h	PID(2): Parameter ID	Spansion Manufacturer ID = 01h
	19h	00h	PID(2): Serial Flash Properties Minor Revisions	Spansion Serial Flash Properties Revision 1.0
	1Ah	01h	PID(2): Serial Flash Properties Major Revisions	
	1Bh	00h	PID(2): Parameter Length	00h = Not implemented
Parameter Header 6	1Ch	A4h	PID(2): Address of Parameter Table (A7-A0)	PID(2) Table Address = 0000A4h
	1Dh	00h	PID(2): Address of Parameter Table (A15-A8)	
	1Eh	00h	PID(2): Address of Parameter Table (A23-A16)	
	1Fh	FFh	Reserved	
Reserved	20h to 7Fh	FFh	Reserved	
JEDEC Flash Parameters 1	80h	E5h	Bits 7:5 = unused = 111b Bits 4:3 = Target flash has nonvolatile status bit and does not require status register to be written on every power on to allow writes and erases = 00b Bit 2 = Program Buffer > 64 bytes = 1 Bits 1:0 = Uniform 4kB erase = 01b	Start of SFDP JEDEC parameter
	81h	20h	4 kbyte Erase Opcode	
	82h	F1h	Bit[7] = 1 Reserved Bit[6] = 1 Supports Quad Out Read (1-1-4) Bit[5] = 1 Supports Quad I/O Read (1-4-4) Bit[4] = 1 Supports Dual I/O Read (1-2-2) Bit[3] = 0 Dual Transfer Rate not Supported Bit[2:1] = 00 3-byte/24-bit Addressing Bit[0] = 1 Supports Single Input Dual Output	Read Command Support
	83h	FFh	Reserved	

Table 7.3 Serial Flash Discoverable Parameter Definition Table (Sheet 2 of 2)

DWORD	Byte Address	Data	Description	Comment
JEDEC Flash Parameters 2	84h	FFh	16 Megabits = 00FFFFFFh 32 Megabits = 01FFFFFFh 64 Megabits = 02FFFFFFh	Flash Size in Bits
	85h	FFh		
	86h	FFh		
	87h	00h / 01h / 02h		
JEDEC Flash Parameters 3	88h	44h	Bit[7:5] = 010 2 cycles of Mode Bits are needed Bit[4:0] = 00100 4 Dummy cycles are needed	Fast Read Quad I/O Default Setting
	89h	EBh	(1-4-4) Quad I/O Fast Read Opcode	
	8Ah	08h	Bit[7:5] = 000 No Mode cycles are needed Bit[4:0] = 01000 8 Dummy cycles are needed	Fast Read Quad Output Default Setting
	8Bh	6Bh	(1-1-4) Quad Output Fast Read Opcode	
JEDEC Flash Parameters 4	8Ch	08h	Bit[7:5] = 000 No Mode cycles are needed Bit[4:0] = 01000 8 Dummy cycles are needed	Fast Read Dual Output Default Setting
	8Dh	3Bh	(1-1-2) Dual Output Fast Read Opcode	
	8Eh	80h	Bit[7:5] = 100 4 Mode cycles are needed Bit[4:0] = 00000 No Dummy cycles are needed	Fast Read Dual I/O Default Setting
	8Fh	BBh	(1-2-2) Dual I/O Fast Read Opcode	
JEDEC Flash Parameters 5	90h	EEh	Bit[31:5]= 1 Reserved Bit[4] = 0 (4-4-4) Quad All Read Not Supported Bit[3:1] = 1 Reserved Bit[0] = 0 (2-2-2) Dual All Read Not Supported	Uniform Width Protocol Support
	91h	FFh		
	92h	FFh		
	93h	FFh		
JEDEC Flash Parameters 6	94h	FFh	Reserved	Dual All Read Parameters Reserved
	95h	FFh	Reserved	
	96h	FFh	Bit[7:5] = 111 Mode cycles needed Bit[4:0] = 11111 Dummy cycles needed	
	97h	FFh	(2-2-2) Dual All Read Command not supported = FFh	
JEDEC Flash Parameters 7	98h	FFh	Reserved	Quad All Read Parameters Reserved
	99h	FFh	Reserved	
	9Ah	FFh	Bit[7:5] = 111 Mode cycles needed Bit[4:0] = 11111 Dummy cycles needed	
	9Bh	FFh	(4-4-4) Quad All Read Command not supported = FFh	
JEDEC Flash Parameters 8	9Ch	0Ch	Sector type 1 size 2^N Bytes = 4kB = 0Ch	Sector Architecture
	9Dh	20h	Sector type 1 instruction	
	9Eh	00h	Sector type 2 size 2^N Bytes = not supported = 00h	
	9Fh	FFh	Sector type 2 instruction = not supported = FFh	
JEDEC Flash Parameters 9	A0h	00h	Sector type 3 size 2^N Bytes = not supported = 00h	
	A1h	FFh	Sector type 3 instruction = not supported = FFh	
	A2h	00h	Sector type 4 size 2^N Bytes = not supported = 00h	
	A3h	FFh	Sector type 4 instruction = not supported = FFh	
	A4h to FFh	FFh	Reserved	

Note:
1. PID(x) = Parameter Identification Table (x).

7.4 Status Registers

Status Register-1 (SR1) and Status Register-2 (SR2) can be used to provide status on the availability of the flash memory array, if the device is write enabled or disabled, the state of write protection, Quad SPI setting, and Security Register lock status.

SR1 and SR2 contain non-volatile bits in locations SR1[7:2] and SR2[6:0] that control sector protection, OTP Register Protection, Status Register Protection, and Quad mode. Bit locations SR2[7], SR1[1], and SR1[0] are read only volatile bits for write enable, and busy status; these are updated by the memory control logic. The SR1[1] write enable bit is set only by the Write Enable (06h) command and cleared by the memory control logic when an embedded operation is completed.

Write access to the non-volatile Status Register bits is controlled by the state of the non-volatile Status Register Protect bits SR1[7] and SR2[0] (SRP0, SRP1), the Write Enable command (06h) preceding a Write Status Registers command, and while Quad mode is not enabled, the WP# pin.

A volatile version of bits SR2[6], SR2[1], and SR1[7:2] that control sector protection and Quad Mode are used to control the behavior of these features after power up. During power up these volatile bits are loaded from the non-volatile version of the Status Register bits. The Write Enable for Volatile Status Register (50h) command can be used to write these volatile bits when the command is followed by a Write Status Registers (01h) command. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits.

Write access to the volatile SR1 and SR2 Status Register bits is controlled by the state of the non-volatile Status Register Protect bits SR1[7] and SR2[0] (SRP0, SRP1), the Write Enable for Volatile Status Register command (50h) preceding a Write Status Registers command, and while Quad mode is not enabled, the WP# pin.

Status Register-3 (SR3) is used to configure and provide status on the variable read latency, and Quad IO wrapped read features.

Write access to the volatile SR3 Status Register bits is controlled by Write Enable for Volatile Status Register command (50h) preceding a Write Status Register command. The SRP bits do not protect SR3.

Table 7.4 Status Register-1 (SR1)

Bits	Field Name	Function	Type	Default State	Description
7	SRP0	Status Register Protect 0	Non-volatile and volatile versions	0	0 = WP# input has no effect or Power Supply Lock Down mode 1 = WP# input can protect the Status Register or OTP Lock Down See Table 7.9 on page 48.
6	SEC	Sector / Block Protect		0	0 = BP2-BP0 protect 64-kB blocks 1 = BP2-BP0 protect 4-kB sectors See Table 7.7 and Table 7.8 for protection ranges.
5	TB	Top / Bottom Protect		0	0 = BP2-BP0 protect from the Top down 1 = BP2-BP0 protect from the Bottom up See Table 7.7 and Table 7.8 for protection ranges
4	BP2	Block Protect Bits		0	000b = No protection See Table 7.7 and Table 7.8 for protection ranges.
3	BP1			0	
2	BP0			0	
1	WEL	Write Enable Latch	Volatile, Read only	0	0 = Not Write Enabled, no embedded operation can start 1 = Write Enabled, embedded operation can start
0	BUSY	Embedded Operation Status	Volatile, Read only	0	0 = Not Busy, no embedded operation in progress 1 = Busy, embedded operation in progress

Table 7.5 Status Register-2 (SR2)

Bits	Field Name	Function	Type	Default State	Description
7	RFU	Reserved		0	Reserved for Future Use
6	CMP	Complement Protect	Non-volatile and volatile versions	0	0 = Normal Protection Map 1 = Inverted Protection Map See Table 7.7 and Table 7.8 for protection ranges.
5	LB3	Security Register Lock Bits	OTP	0	OTP Lock Bits 3:0 for Security Registers 3:0 0 = Security Register not protected 1 = Security Register protected Security register 0 contains the Serial Flash Discoverable Parameters and is always programmed and locked by Spansion.
4	LB2			0	
3	LB1			0	
2	LB0 (1)			1	
1	QE	Quad Enable	Non-volatile and volatile versions	0	0 = Quad Mode Not Enabled, the WP# pin and HOLD# are enabled 1 = Quad Mode Enabled, the IO2 and IO3 pins are enabled, and WP# and HOLD# functions are disabled
0	SRP1	Status Register Protect 1		0	0 = SRP0 selects whether WP# input has effect on protection of the Status Register 1 = SRP0 selects Power Supply Lock Down or OTP Lock Down mode See Table 7.9 on page 48.

Note:
1. LB0 value should be considered don't care for read. This bit is set to 1.

Table 7.6 Status Register-3 (SR3)

Bits	Field Name	Function	Type	Default State	Description
7	RFU	Reserved		0	Reserved for Future Use
6	W6	Burst Wrap Length	Volatile	1	00 = 8-byte wrap. Data read starts at the initial address and wraps within an aligned 8-byte boundary 01 = 16-byte wrap. Data read starts at the initial address and wraps within an aligned 16-byte boundary. 10 = 32-byte wrap. Data read starts at the initial address and wraps within an aligned 32-byte boundary. 11 = 64-byte wrap. Data read starts at the initial address and wraps within an aligned 64-byte boundary.
5	W5			1	
4	W4	Burst Wrap Enable		1	0 = Wrap Enabled 1 = Wrap Disabled
3	Latency Control (LC)	Variable Read Latency Control		0	Defines the number of read latency cycles in Fast Read, Dual Out, Quad Out, Dual IO, and Quad IO commands. Binary values for 1 to 15 latency cycles. A value of zero disables the variable latency mode.
2				0	
1				0	
0				0	

7.4.1 BUSY

BUSY is a read only bit in the Status Register (SR1[0]) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Registers or Erase/Program Security Register command. During this time the device will ignore further commands except for the Read Status Register command (see t_W, t_{PP}, t_{SE}, t_{BE}, and t_{CE} in Section 5.7, *AC Electrical Characteristics* on page 30). When the write status/security register command has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further commands.

7.4.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the Status Register (SR1[1]) that is set to 1 after executing a Write Enable Command. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following commands: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Registers, Erase Security Register and Program Security Register. The WEL status bit is cleared to 0 even when a program or erase operation is prevented by the block protection bits.

7.4.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the Status Register (SR1[4:2]) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Registers Command (see t_W in Section 5.7, *AC Electrical Characteristics* on page 30). All, none or a portion of the memory array can be protected from Program and Erase commands (see Section 7.4.7, *Block Protection Maps* on page 46). The factory default setting for the Block Protection Bits is 0 (none of the array is protected.)

7.4.4 Top/Bottom Block Protect (TB)

The non-volatile Top/Bottom bit (TB SR1[5]) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in Section 7.4.7, *Block Protection Maps* on page 46. The factory default setting is TB=0. The TB bit can be set with the Write Status Registers Command depending on the state of the SRP0, SRP1 and WEL bits.

7.4.5 Sector/Block Protect (SEC)

The non-volatile Sector/Block Protect bit (SEC SR1[6]) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4-kB Sectors (SEC=1) or 64-kB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in Section 7.4.7, *Block Protection Maps* on page 46. The default setting is SEC=0.

7.4.6 Complement Protect (CMP)

The Complement Protect bit (CMP SR2[6]) is a non-volatile read/write bit in the Status Register (SR2[6]). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 4-kB sector can be protected while the rest of the array is not; when CMP=1, the top 4-kB sector will become unprotected while the rest of the array become read-only. Please refer to Section 7.4.7, *Block Protection Maps* on page 46 for details. The default setting is CMP=0.

7.4.7 Block Protection Maps

Table 7.7 FL116K Block Protection (CMP = 0)

Status Register (1)					S25FL116K (16 Mbit) Block Protection (CMP=0) (2)			
SEC	TB	BP2	BP1	BP0	Protected Block(s)	Protected Addresses	Protected Density	Protected Portion
X	X	0	0	0	None	None	None	None
0	0	0	0	1	31	1F0000h – 1FFFFFh	64 kB	Upper 1/32
0	0	0	1	0	30 and 31	1E0000h – 1FFFFFh	128 kB	Upper 1/16
0	0	0	1	1	28 thru 31	1C0000h – 1FFFFFh	256 kB	Upper 1/8
0	0	1	0	0	24 thru 31	180000h – 1FFFFFh	512 kB	Upper 1/4
0	0	1	0	1	16 thru 31	100000h – 1FFFFFh	1 MB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64 kB	Lower 1/32
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128 kB	Lower 1/16
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256 kB	Lower 1/8
0	1	1	0	0	0 thru 7	000000h – 07FFFFh	512 kB	Lower 1/4
0	1	1	0	1	0 thru 15	000000h – 0FFFFFh	1 MB	Lower 1/2
X	X	1	1	X	0 thru 31	000000h – 1FFFFFh	2 MB	All
1	0	0	0	1	31	1FF000h – 1FFFFFh	4 kB	Upper 1/512
1	0	0	1	0	31	1FE000h – 1FFFFFh	8 kB	Upper 1/256
1	0	0	1	1	31	1FC000h – 1FFFFFh	16 kB	Upper 1/128
1	0	1	0	X	31	1F8000h – 1FFFFFh	32 kB	Upper 1/64
1	1	0	0	1	0	000000h – 000FFFh	4 kB	Lower 1/512
1	1	0	1	0	0	000000h – 001FFFh	8 kB	Lower 1/256
1	1	0	1	1	0	000000h – 003FFFh	16 kB	Lower 1/128
1	1	1	0	X	0	000000h – 007FFFh	32 kB	Lower 1/64

Notes:

1. *X = don't care.*
2. *If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.*

Table 7.8 FL116K Block Protection (CMP = 1)

Status Register (1)					S25FL116K (16 Mbit) Block Protection (CMP=1) (2)			
SEC	TB	BP2	BP1	BP0	Protected Block(s)	Protected Addresses	Protected Density	Protected Portion
X	X	0	0	0	0 thru 31	000000h – 1FFFFFh	All	All
0	0	0	0	1	0 thru 30	000000h – 1EFFFFh	1,984 kB	Lower 31/32
0	0	0	1	0	0 thru 29	000000h – 1DFFFFh	1,920 kB	Lower 15/16
0	0	0	1	1	0 thru 27	000000h – 1BFFFFh	1,792 kB	Lower 7/8
0	0	1	0	0	0 thru 23	000000h – 17FFFFh	1,536 kB	Lower 3/4
0	0	1	0	1	0 thru 15	000000h – 0FFFFFh	1 MB	Lower 1/2
0	1	0	0	1	1 thru 31	010000h – 1FFFFFh	1,984 kB	Upper 31/32
0	1	0	1	0	2 and 31	020000h – 1FFFFFh	1,920 kB	Upper 15/16
0	1	0	1	1	4 thru 31	040000h – 1FFFFFh	1,792 kB	Upper 7/8
0	1	1	0	0	8 thru 31	080000h – 1FFFFFh	1,536 kB	Upper 3/4
0	1	1	0	1	16 thru 31	100000h – 1FFFFFh	1 MB	Upper 1/2
X	X	1	1	X	None	None	None	None
1	0	0	0	1	0 thru 31	000000h – 1FEFFFh	2,044 kB	Lower 511/512
1	0	0	1	0	0 thru 31	000000h – 1FDFFFh	2,040 kB	Lower 255/256
1	0	0	1	1	0 thru 31	000000h – 1FBFFFh	2,032 kB	Lower 127/128
1	0	1	0	X	0 thru 31	000000h – 1F7FFFh	2,016 kB	Lower 63/64
1	1	0	0	1	0 thru 31	001000h – 1FFFFFh	2,044 kB	Upper 511/512
1	1	0	1	0	0 thru 31	002000h – 1FFFFFh	2,040 kB	Upper 255/256
1	1	0	1	1	0 thru 31	004000h – 1FFFFFh	2,032 kB	Upper 127/128
1	1	1	0	X	0 thru 31	008000h – 1FFFFFh	2,016 kB	Upper 63/64

Notes:

1. *X = don't care.*
2. *If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.*

7.4.8 Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the Status Register (SR2[0] and SR1[7]). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down, or one time programmable (OTP) protection.

Table 7.9 Status Register Protection Bits

SRP1	SRP0	WP#	Status Register	Description
0	0	X	Software Protection	WP# pin has no control. SR1 and SR2 can be written to after a Write Enable command, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When WP# pin is low the SR1 and SR2 are locked and can not be written.
0	1	1	Hardware Unprotected	When WP# pin is high SR1 and SR2 are unlocked and can be written to after a Write Enable command, WEL=1.
1	0	X	Power Supply Lock-Down	SR1 and SR2 are protected and can not be written to again until the next power-down, power-up cycle. (1)
1	1	X	One Time Program (2)	SR1 and SR2 are permanently protected and can not be written.

Notes:

1. *When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.*
2. *The One Time Program feature is available upon special order. Please contact Spansion for details.*
3. *Busy, WEL, and SUS (SR1[1:0] and SR2[7]) are volatile read only status bits that are never affected by the Write Status Registers command.*
4. *The non-volatile version of CMP, QE, SRP1, SRP0, SEC, TB, and BP2-BP0 (SR2[6,1,0] and SR1[6:2]) bits and the OTP LB3-LB0 bits are not writable when protected by the SRP bits and WP# as shown in the table. The non-volatile version of these Status Register bits are selected for writing when the Write Enable (06h) command precedes the Write Status Registers (01h) command.*
5. *The volatile version of CMP, QE, SRP1, SRP0, SEC, TB, and BP2-BP0 (SR2[6,1,0] and SR1[6:2]) bits are not writable when protected by the SRP bits and WP# as shown in the table. The volatile version of these Status Register bits are selected for writing when the Write Enable for volatile Status Register (50h) command precedes the Write Status Registers (01h) command. There is no volatile version of the LB3-LB0 bits and these bits are not affected by a volatile Write Status Registers command.*
6. *The volatile SR3 bits are not protected by the SRP bits and may be written at any time by volatile (50h) Write Enable command preceding the Write Status Registers (01h) command.*

7.4.9 Security Register Lock Bits (LB3, LB2, LB1, LB0)

The Security Register Lock Bits (LB3, LB2, LB1, LB0) are non-volatile One Time Program (OTP) bits in Status Register (SR2[5:2]) that provide the write protect control and status to the Security Registers. The default state of LB[3:1] is 0, Security Registers 1 to 3 are unlocked. LB[3:1] can be set to 1 individually using the Write Status Registers command. LB[3:1] are One Time Programmable (OTP), once it's set to 1, the corresponding 256-byte Security Register will become read-only permanently.

Security Register 0 is programmed with the SFDP parameters and LB0 is programmed to 1 by Spansion.

7.4.10 Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read/write bit in the Status Register (SR2[1]) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default), the WP# pin and HOLD# are enabled. When the QE bit is set to a 1, the Quad IO2 and IO3 pins are enabled, and WP# and HOLD# functions are disabled.

Note: If the WP# or HOLD# pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

7.4.11 Latency Control (LC)

Status Register-3 provides bits (SR3[3:0]) to select the number of read latency cycles used in each Fast Read command. The Read Data command is not affected by the latency code. The binary value of this field selects from 1 to 15 latency cycles. The zero value selects the legacy number of latency cycles used in prior generation FL-K family devices. The default is 0 cycles to provide backward compatibility to legacy devices. The Latency Control bits may be set to select a number of read cycles optimized for the frequency in use. If the number of latency cycles is not sufficient for the operating frequency, invalid data will be read.

Table 7.10 Latency Cycles Versus Frequency

Latency Control	Read Command Maximum Frequency (MHz)				
	FAST READ	DUAL OUTPUT	DUAL I/O	QUAD OUTPUT	QUAD I/O
0 (legacy read latency)	108 (8 dummy)	108 (8 dummy)	88 (4 mode, 0 dummy)	108 (8 dummy)	78 (2 mode, 4 dummy)
1	50	50	94	43	49
2	95	85	105	56	59
3	105	95	108	70	69
4	108	105	108	83	78
5	108	108	108	94	86
6	108	108	108	105	95
7	108	108	108	108	105
8	108	108	108	108	108
9	108	108	108	108	108
10	108	108	108	108	108
11	108	108	108	108	108
12	108	108	108	108	108
13	108	108	108	108	108
14	108	108	108	108	108
15	108	108	108	108	108

Notes:

1. *SCK frequency > 108 MHz SIO, 108 MHz DIO, or 108 MHz QIO is not supported by this family of devices.*
2. *The Dual I/O and Quad I/O command protocols include Continuous Read Mode bits following the address. The clock cycles for these bits are not counted as part of the latency cycles shown in the table. Example: the legacy Dual I/O command has 4 Continuous Read Mode bits following the address and no additional dummy cycles. Therefore, the legacy Dual I/O command without additional read latency is supported only up to the frequency shown in the table for a read latency of 0 cycles. By increasing the variable read latency the frequency of the Dual I/O command can be increased to allow operation up to the maximum supported 108 MHz DIO frequency.*

7.4.12 Burst Wrap Enable (W4)

Status Register-3 provides a bit (SR3[4]) to enable a read with wrap option for the Quad I/O Read command. When SR3[4]=1, the wrap mode is not enabled and unlimited length sequential read is performed. When SR3[4]=0, the wrap mode is enabled and a fixed length and aligned group of 8, 16, 32, or 64 bytes will be read starting at the byte address provided by the Quad I/O Read command and wrapping around at the group alignment boundary.

7.4.13 Burst Wrap Length (W6, W5)

Status Register-3 provides bits (SR3[1:0]) to select the alignment boundary at which reading will wrap to perform a cache line fill. Reading begins at the initial byte address of a Fast Read Quad IO command, then sequential bytes are read until the selected boundary is reached. Reading then wraps to the beginning of the selected boundary. This enables critical word first cache line refills. The wrap point can be aligned on 8-, 16-, 32-, or 64-byte boundaries.

7.5 Device Identification

7.5.1 Legacy Device Identification Commands

Three legacy commands are supported to access device identification that can indicate the manufacturer, device type, and capacity (density). The returned data bytes provide the information as shown in Table 7.11.

Table 7.11 Device Identification

Device OPN	Instruction	Data 1	Data 2	Data 3
S25FL116K	ABh	Device ID = 14h	-	-
	90h	Manufacturer ID = 01h	Device ID = 14h	-
	9Fh	Manufacturer ID = 01h	Device Type = 40h	Capacity = 15h

Note:

1. *The 90h instruction is followed by an address. Address = 0 selects Manufacturer ID as the first returned data as shown in the table. Address = 1 selects Device ID as the first returned data followed by Manufacturer ID.*

7.5.2 Serial Flash Discoverable Parameters (SFDP)

A Read SFDP (5Ah) command to read a JEDEC standard (JESD216) defined device information structure is supported. The information is stored in Security Register 0 and described in *Security Register 0 - Serial Flash Discoverable Parameters (SFDP)* on page 40.

8. Functional Description

8.1 SPI Operations

8.1.1 Standard SPI Commands

The S25FL116K is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Standard SPI commands use the SI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The SO output pin is used to read data or status from the device on the falling edge CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.

8.1.2 Dual SPI Commands

The S25FL116K supports Dual SPI operation when using the “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)” commands. These commands allow data to be transferred to or from the device at two to three times the rate of ordinary serial flash devices. The Dual SPI Read commands are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI commands, the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

8.1.3 Quad SPI Commands

The S25FL116K supports Quad SPI operation when using the “Fast Read Quad Output (6Bh)”, and “Fast Read Quad I/O (EBh)” commands. These commands allow data to be transferred to or from the device four to six times the rate of ordinary serial flash. The Quad Read commands offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI commands the SI and SO pins become bidirectional IO0 and IO1, and the WP# and HOLD# pins become IO2 and IO3 respectively. Quad SPI commands require the non-volatile or volatile Quad Enable bit (QE) in Status Register-2 to be set.

8.1.4 Hold Function

For Standard SPI and Dual SPI operations, the HOLD# (IO3) signal allows the device interface operation to be paused while it is actively selected (when CS# is low). The Hold function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, if the page buffer is only partially written when a priority interrupt requires use of the SPI bus. The Hold function is only available for standard SPI and Dual SPI operation, not during Quad SPI.

To initiate a Hold condition, the device must be selected with CS# low. A Hold condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the Hold condition will activate after the next falling edge of CLK. The Hold condition will terminate on the rising edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the Hold condition will terminate after the next falling edge of CLK. During a Hold condition, the Serial Data Output, (SO) or IO0 and IO1, are high impedance and Serial Data Input, (SI) or IO0 and IO1, and Serial Clock (CLK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the Hold operation to avoid resetting the internal logic state of the device.

8.2 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the S25FL116K provides several means to protect the data from inadvertent program or erase.

8.2.1 Write Protect Features

- Device resets when V_{CC} is below threshold
- Time delay write disable after Power-Up
- Write enable/disable commands and automatic write disable after erase or program
- Command length protection
  - All commands that Write, Program or Erase must complete on a byte boundary (CS# driven high after a full 8 bits have been clocked) otherwise the command will be ignored
- Software and Hardware write protection using Status Register control
  - WP# input protection
  - Lock Down write protection until next power-up
  - One Time Program (OTP) write protection
- Write Protection using the Deep Power-down command

Upon power-up or at power-down, the S25FL116K will maintain a reset condition while V_{CC} is below the threshold value of VWI, (see Figure 5.5, *Power-Up Timing and Voltage Levels* on page 29). While reset, all operations are disabled and no commands are recognized. During power-up and after the V_{CC} voltage exceeds VWI, all program and erase related commands are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Registers commands. Note that the chip select pin (CS#) must track the V_{CC} supply level at power-up until the V_{CC}-min level and t_{VSL} time delay is reached. If needed a pull-up resistor on CS# can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable command must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Registers command will be accepted. After completing a program, erase or write command the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled main flash array write protection is facilitated using the Write Status Registers command to write the Status Register Protect (SRP0, SRP1) and Block Protect (CMP, SEC,TB, BP2, BP1 and BP0) bits.

The BP method allows a portion as small as 4-kB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (WP#) pin, changes to the Status Register can be enabled or disabled under hardware control. See *Status Registers* on page 43. for further information.

Additionally, the Deep-Power-Down (DPD) command offers an alternative means of data protection as all commands are ignored during the DPD state, except for the Release from Deep-Power-Down (RES ABh) command. Thus, preventing any program or erase during the DPD state.

8.3 Status Registers

The Read and Write Status Registers commands can be used to provide status and control of the flash memory device.

9. Commands

The command set of the S25FL116K is fully controlled through the SPI bus (see Table 9.1 to Table 9.3 on page 54). Commands are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked into the SI input provides the instruction code. Data on the SI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Commands vary in length from a single byte to several bytes. Each command begins with an instruction code and may be followed by address bytes, a mode byte, read latency (dummy / don't care) cycles, or data bytes. Commands are completed with the rising edge of edge CS#. Clock relative sequence diagrams for each command are included in the command descriptions. All read commands can be completed after any data bit. However, all commands that Write, Program must complete on a byte boundary (CS# driven high after a full 8 bits have been clocked) otherwise the command will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, all commands except for Read Status Register commands will be ignored until the program or erase cycle has completed. When the Status Register is being written, all commands except for Read Status Register will be ignored until the Status Register write operation has completed.

Table 9.1 Command Set (Configuration, Status, Erase, Program Commands(1))

Command Name	BYTE 1 (Instruction)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Read Status Register-1	05h	SR1[7:0] (2)(4)				
Read Status Register-2	35h	SR2[7:0] (2)(4)				
Read Status Register-3	33h	SR3[7:0] (2)				
Write Enable	06h					
Write Enable for Volatile Status Register	50h					
Write Disable	04h					
Write Status Registers	01h	SR1[7:0]	SR2[7:0]	SR3[7:0]		
Set Burst with Wrap	77h	xxh	xxh	xxh	SR3[7:0] (3)	
Page Program	02h	A23–A16	A15–A8	A7–A0	D7–D0	
Sector Erase (4 kB)	20h	A23–A16	A15–A8	A7–A0		
Block Erase (64 kB)	D8h	A23–A16	A15–A8	A7–A0		
Chip Erase	C7h/60h					

Notes:

1. *Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "()" indicate data being read from the device on the SO pin.*
2. *Status Register contents will repeat continuously until CS# terminates the command.*
3. *Set Burst with Wrap Input format to load SR3. See Table 7.6 on page 44.*
   IO0 = x, x, x, x, x, W4, x]
   IO1 = x, x, x, x, x, W5, x]
   IO2 = x, x, x, x, x, W6 x]
   IO3 = x, x, x, x, x, x,x
4. *When changing the value of any single bit, read all other bits and rewrite the same value to them.*

Table 9.2 Command Set (Read Commands)

Command Name	BYTE 1 (Instruction)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Read Data	03h	A23–A16	A15–A8	A7–A0	(D7–D0, …)	
Fast Read	0Bh	A23–A16	A15–A8	A7–A0	dummy	(D7–D0, …)
Fast Read Dual Output	3Bh	A23–A16	A15–A8	A7–A0	dummy	(D7–D0, …) (1)
Fast Read Quad Output	6Bh	A23–A16	A15–A8	A7–A0	dummy	(D7–D0, …) (3)
Fast Read Dual I/O	BBh	A23–A8 (2)	A7–A0, M7–M0 (2)	(D7–D0, …) (1)		
Fast Read Quad I/O	EBh	A23–A0, M7–M0 (4)	(x,x,x,x, D7–D0, …) (5)	(D7–D0, …) (3)		
Continuous Read Mode Reset (6)	FFh	FFh				

Notes:

1. *Dual Output data*
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
2. *Dual Input Address*
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
3. *Quad Output Data*
   IO0 = (D4, D0, …..)
   IO1 = (D5, D1, …..)
   IO2 = (D6, D2, …..)
   IO3 = (D7, D3, …..)
4. *Quad Input Address*
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3
5. *Fast Read Quad I/O Data*
   IO0 = (x, x, x, x, D4, D0, …..)
   IO1 = (x, x, x, x, D5, D1, …..)
   IO2 = (x, x, x, x, D6, D2, …..)
   IO3 = (x, x, x, x, D7, D3, …..)
6. *This command is recommended when using the Dual or Quad "Continuous Read Mode" feature. See Section 9.3.8 and Section 9.3.8 on page 66 for more information.*

Table 9.3 Command Set (ID, Security Commands)

Command Name	BYTE 1 (Instruction)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Deep Power-down	B9h					
Release Power down / Device ID	ABh	dummy	dummy	dummy	Device ID (1)	
Manufacturer/ Device ID (2)	90h	dummy	dummy	00h	Manufacturer	Device ID
JEDEC ID	9Fh	Manufacturer	Memory Type	Capacity		
Read SFDP Register	5Ah	00h	00h	A7–A0	dummy	(D7–D0, …)
Read Security Registers (3)	48h	A23–A16	A15–A8	A7–A0	dummy	(D7–D0, …)
Erase Security Registers (3)	44h	A23–A16	A15–A8	A7–A0		
Program Security Registers (3)	42h	A23–A16	A15–A8	A7–A0	D7–D0, …	

Notes:

1. *The Device ID will repeat continuously until /CS terminates the command.*
2. *See Section 7.5.1, Legacy Device Identification Commands on page 50 for Device ID information. The 90h instruction is followed by an address. Address = 0 selects Manufacturer ID as the first returned data as shown in the table. Address = 1 selects Device ID as the first returned data followed by Manufacturer ID.*
3. *Security Register Address:*
   Security Register 0: A23-16 = 00h; A15-8 = 00h; A7-0 = byte address
   Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address
   Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte address
   Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address

   Security Register 0 is used to store the SFDP parameters and is always programmed and locked by Spansion.

9.1 Configuration and Status Commands

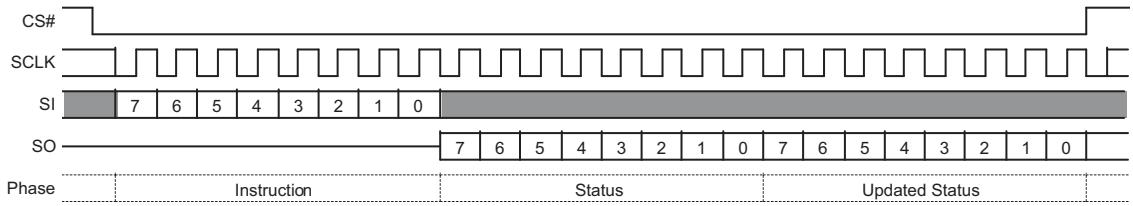
9.1.1 Read Status Registers (05h), (35h), (33h)

The Read Status Register commands allow the 8-bit Status Registers to be read. The command is entered by driving CS# low and shifting the instruction code “05h” for Status Register-1, “35h” for Status Register-2, or 33h for Status Register-3, into the SI pin on the rising edge of CLK. The Status Register bits are then shifted out on the SO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 9.1. The Status Register bits are shown in Section 7.4, *Status Registers* on page 43.

The Read Status Register-1 (05h) command may be used at any time, even while a Program, Erase or Write Status Registers cycle is in progress. This allows the BUSY status bit to be checked to determine when the operation is complete and if the device can accept another command. The Read Status Register-2 (35h), and Read Status Registers (33h) may be used only when the device is in standby, not busy with an embedded operation.

Status Registers can be read continuously as each repeated data output delivers the updated current value of each Status Register. Example: using the instruction code “05h” for Read Status Register-1, the first output of eight bits may show the device is busy, SR1[0]=1. By continuing to hold CS# low, the updated value of SR1 will be shown in the next byte output. This repeated reading of SR1can continue until the system detects the Busy bit has changed back to ready status in one of the status bytes being read out. The Read Status Register commands are completed by driving CS# high.

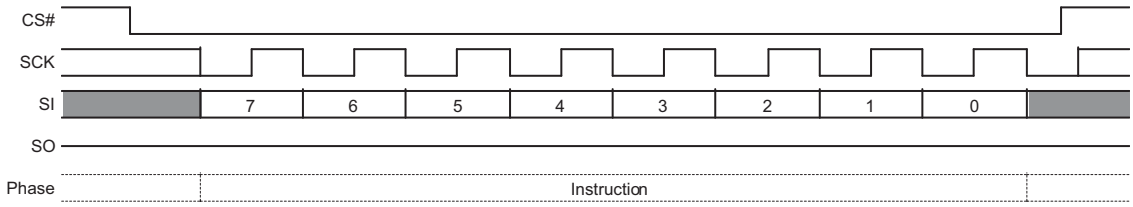
Figure 9.1 Read Status Register Command Sequence Diagram



9.1.2 Write Enable (06h)

The Write Enable command (Figure 9.2) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Registers and Erase/Program Security Registers command. The Write Enable command is entered by driving CS# low, shifting the instruction code “06h” into the Data Input (SI) pin on the rising edge of CLK, and then driving CS# high.

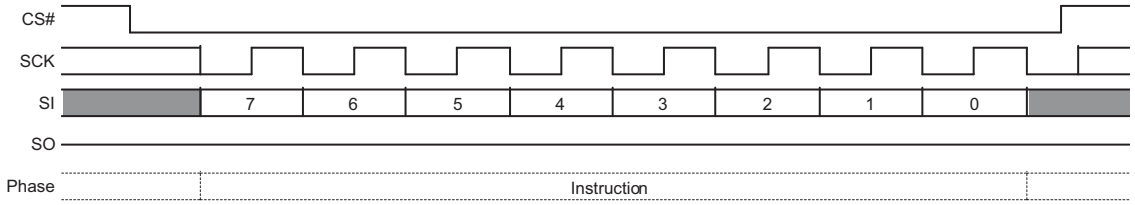
Figure 9.2 Write Enable (WREN 06h) Command Sequence



9.1.3 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in Section 7.4, *Status Registers* on page 43 can also be written to as volatile bits. During power up reset, the non-volatile Status Register bits are copied to a volatile version of the Status Register that is used during device operation. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile version of the Status Register bits, the Write Enable for Volatile Status Register (50h) command must be issued and immediately followed by the Write Status Registers (01h) command. Write Enable for Volatile Status Register command (Figure 9.3) will not set the Write Enable Latch (WEL) bit, it is only valid for the next following Write Status Registers command, to change the volatile Status Register bit values.

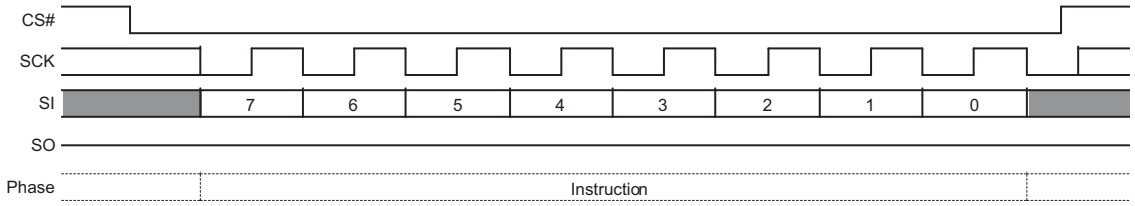
Figure 9.3 Write Enable for Volatile Status Register Command Sequence



9.1.4 Write Disable (04h)

The Write Disable command resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable command is entered by driving CS# low, shifting the instruction code “04h” into the SI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Registers, Erase/Program Security Registers, Page Program, Sector Erase, Block Erase and Chip Erase commands.

Figure 9.4 Write Disable (WRDI 04h) Command Sequence



9.1.5 Write Status Registers (01h)

The Write Status Registers command allows the Status Registers to be written. Only non-volatile Status Register bits SRP0, SEC, TB, BP2, BP1, BP0 (SR1[7:2]) CMP, LB3, LB2, LB1, QE, SRP1 (SR2[6:0]), and the volatile bits SR3[6:0] can be written. All other Status Register bit locations are read-only and will not be affected by the Write Status Registers command. LB3-0 are non-volatile OTP bits; once each is set to 1, it can not be cleared to 0. The Status Register bits are shown in Section 7.4, *Status Registers* on page 43. Any reserved bits should only be written to their default value.

To write non-volatile Status Register bits, a standard Write Enable (06h) command must previously have been executed for the device to accept the Write Status Registers Command (Status Register bit WEL must equal 1). Once write enabled, the command is entered by driving CS# low, sending the instruction code “01h”, and then writing the Status Register data bytes as illustrated in Figure 9.5.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) command must have been executed prior to the Write Status Registers command (Status Register bit WEL remains 0). However, SRP1 and LB3, LB2, LB1, LB0 can not be changed because of the OTP protection for these bits. Upon power off, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored when power on again.

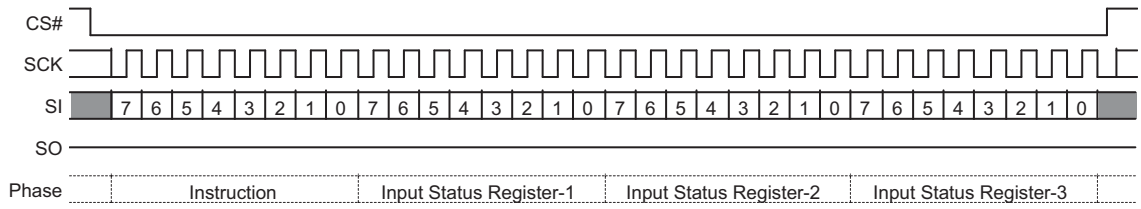
To complete the Write Status Registers command, the CS# pin must be driven high after the eighth bit of a data value is clocked in (CS# must be driven high on an 8-bit boundary). If this is not done the Write Status Registers command will not be executed. If CS# is driven high after the eighth clock the CMP and QE bits will be cleared to 0 if the SRP1 bit is 0. The SR2 bits are unaffected if SRP1 is 1. If CS# is driven high after the eighth or sixteenth clock, the SR3 bits will not be affected.

During non-volatile Status Register write operation (06h combined with 01h), after CS# is driven high at the end of the Write Status Registers command, the self-timed Write Status Registers operation will commence for a time duration of t_W (see Section 5.7, *AC Electrical Characteristics* on page 30). While the Write Status Registers operation is in progress, the Read Status Register command may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Registers operation and a 0 when the operation is finished and ready to accept other commands again. After the Write Status Registers operation has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h), after CS# is driven high at the end of the Write Status Registers command, the Status Register bits will be updated to the new values within the time period of t_{SHSL2} (see Section 5.7, *AC Electrical Characteristics* on page 30). BUSY bit will remain 0 during the Status Register bit refresh period.

Refer to Section 7.4, *Status Registers* on page 43 for detailed Status Register Bit descriptions.

Figure 9.5 Write Status Registers Command Sequence Diagram



9.2 Program and Erase Commands

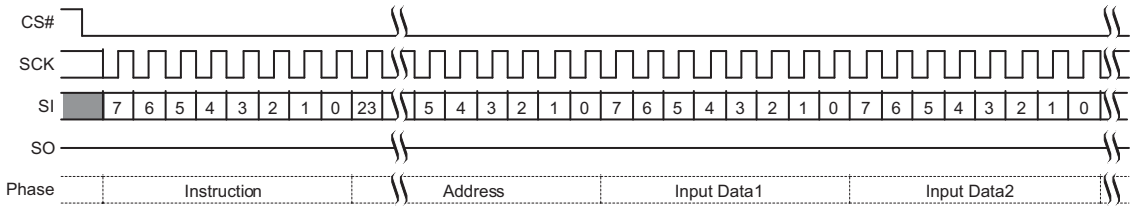
9.2.1 Page Program (02h)

The Page Program command allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable command must be executed before the device will accept the Page Program Command (Status Register bit WEL= 1). The command is initiated by driving the CS# pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the SI pin. The CS# pin must be held low for the entire length of the command while data is being sent to the device. The Page Program command sequence is shown in Figure 9.6, *Page Program Command Sequence* on page 58.

If an entire 256-byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceed the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase commands, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program command will not be executed. After CS# is driven high, the self-timed Page Program command will commence for a time duration of t_{PP} (Section 5.7, *AC Electrical Characteristics* on page 30). While the Page Program cycle is in progress, the Read Status Register command may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program command will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

Figure 9.6 Page Program Command Sequence

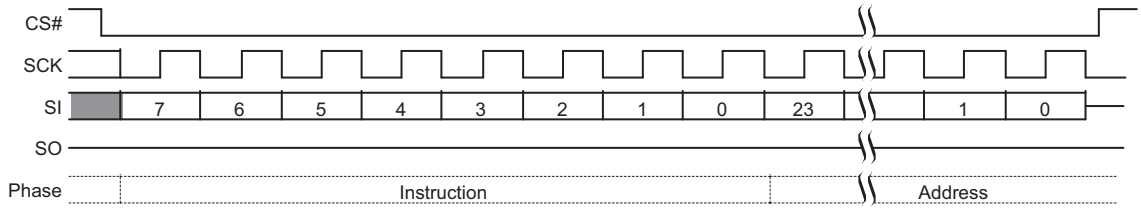


9.2.2 Sector Erase (20h)

The Sector Erase command sets all memory within a specified sector (4 kbytes) to the erased state of all 1's (FFh). A Write Enable command must be executed before the device will accept the Sector Erase Command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the instruction code "20h" followed a 24-bit sector address (A23-A0) See *Supply and Signal Ground (V_{SS})* on page 15. The Sector Erase command sequence is shown in Figure 9.7 on page 59.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase command will not be executed. After CS# is driven high, the self-timed Sector Erase command will commence for a time duration of t_{SE}. Section 5.7, *AC Electrical Characteristics* on page 30 While the Sector Erase cycle is in progress, the Read Status Register command may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase command will not be executed if the addressed sector is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

Figure 9.7 Sector Erase Command Sequence

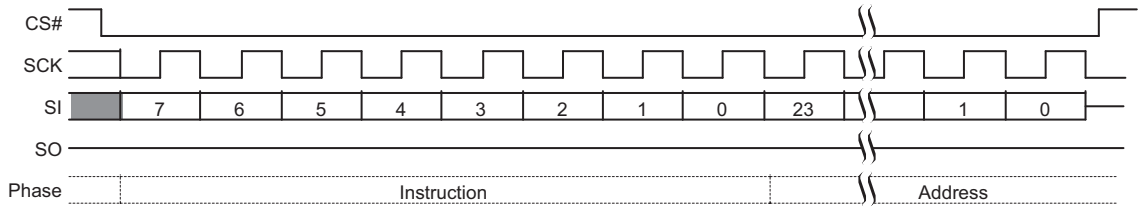


9.2.3 64-kB Block Erase (D8h)

The Block Erase command sets all memory within a specified block (64 kbytes) to the erased state of all 1s (FFh). A Write Enable command must be executed before the device will accept the Block Erase Command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the instruction code "D8h" followed a 24-bit block address (A23-A0) See *Supply and Signal Ground (V_{SS})* on page 15. The Block Erase command sequence is shown in Figure 9.8.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase command will not be executed. After CS# is driven high, the self-timed Block Erase command will commence for a time duration of t_{BE} (see Section 5.7, *AC Electrical Characteristics* on page 30). While the Block Erase cycle is in progress, the Read Status Register command may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase command will not be executed if the addressed sector is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Section 7.4, *Status Registers* on page 43).

Figure 9.8 64 kB Block Erase Command Sequence

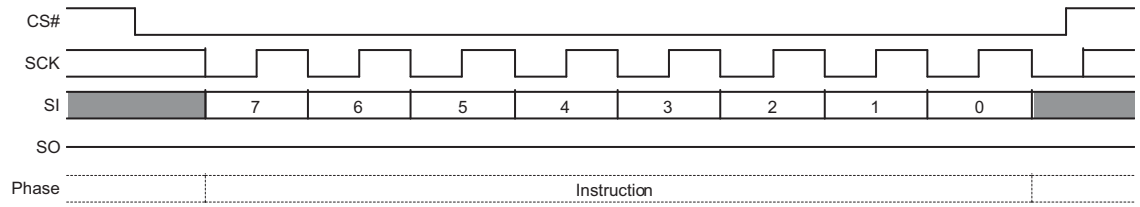


9.2.4 Chip Erase (C7h / 60h)

The Chip Erase command sets all memory within the device to the erased state of all 1's (FFh). A Write Enable command must be executed before the device will accept the Chip Erase Command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the instruction code "C7h" or "60h". The Chip Erase command sequence is shown in Figure 9.9.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase command will not be executed. After CS# is driven high, the self-timed Chip Erase command will commence for a time duration of t_{CE} (Section 5.7, *AC Electrical Characteristics* on page 30). While the Chip Erase cycle is in progress, the Read Status Register command may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other commands again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase command will not be executed if any page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Section 7.4, *Status Registers* on page 43).

Figure 9.9 Chip Erase Command Sequence



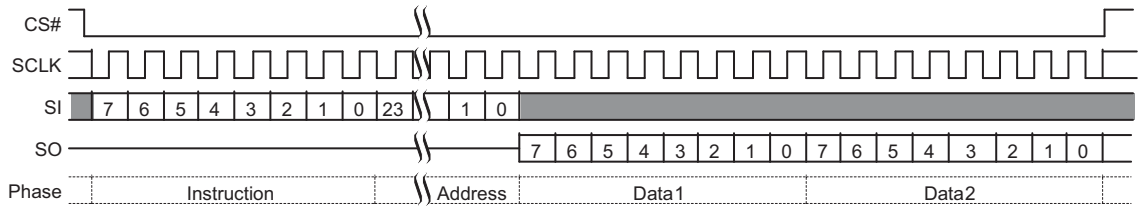
9.3 Read Commands

9.3.1 Read Data (03h)

The Read Data command allows one or more data bytes to be sequentially read from the memory. The command is initiated by driving the CS# pin low and then shifting the instruction code "03h" followed by a 24-bit address (A23-A0) into the SI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the SO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single command as long as the clock continues. The command is completed by driving CS# high.

The Read Data command sequence is shown in Figure 9.10. If a Read Data command is issued while an Erase, Program or Write cycle is in process (BUSY=1) the command is ignored and will not have any effects on the current cycle. The Read Data command allows clock rates from DC to a maximum of f_R (see Section 5.7, *AC Electrical Characteristics* on page 30).

Figure 9.10 Read Data Command Sequence

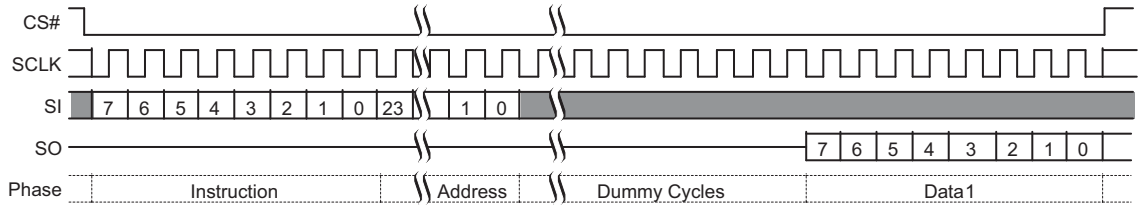


9.3.2 Fast Read (0Bh)

The Fast Read command is similar to the Read Data command except that it can operate at higher frequency than the traditional Read Data command. This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 9.11. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the SI pin is a “don’t care”.

When variable read latency is enabled, the number of dummy cycles is set by the Latency Control value in SR3 to optimize the latency for the frequency in use. See. Table 7.10, *Latency Cycles Versus Frequency* on page 49.

Figure 9.11 Fast Read Command Sequence



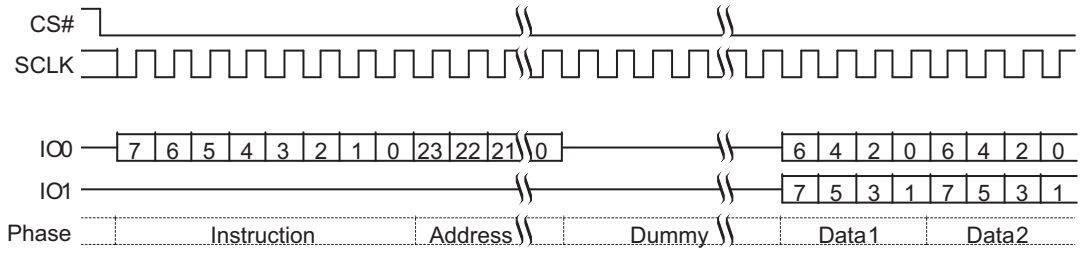
9.3.3 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) command is similar to the standard Fast Read (0Bh) command except that data is output on two pins; IO0 and IO1. This allows data to be transferred from the S25FL116K at twice the rate of standard SPI devices. The Fast Read Dual Output command is ideal for quickly downloading code from flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read command, the Fast Read Dual Output command can operate at higher frequency than the traditional Read Data command. This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 9.12. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO0 pin should be high-impedance prior to the falling edge of the first data out clock.

When variable read latency is enabled, the number of dummy cycles is set by the Latency Control value in SR3 to optimize the latency for the frequency in use. See. Table 7.10, *Latency Cycles Versus Frequency* on page 49.

Figure 9.12 Fast Read Dual Output Command Sequence



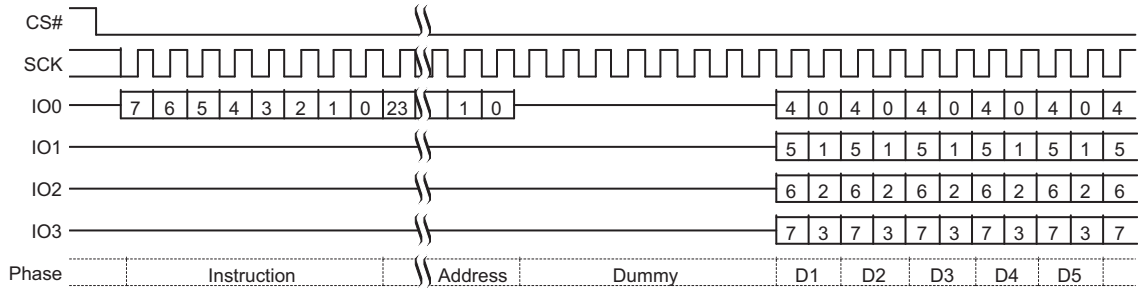
9.3.4 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) command is similar to the Fast Read Dual Output (3Bh) command except that data is output on four pins, IO0, IO1, IO2, and IO3. A Quad enable of Status Register-2 must be executed before the device will accept the Fast Read Quad Output Command (Status Register bit QE must equal 1). The Fast Read Quad Output Command allows data to be transferred from the S25FL116K at four times the rate of standard SPI devices.

The Fast Read Quad Output command can operate at higher frequency than the traditional Read Data command. This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 9.13. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

When variable read latency is enabled, the number of dummy cycles is set by the Latency Control value in SR3 to optimize the latency for the frequency in use. See. Table 7.10, *Latency Cycles Versus Frequency* on page 49.

Figure 9.13 Fast Read Quad Output Command Sequence



9.3.5 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) command allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (3Bh) command but with the capability to input the Address bits (A23-0) two bits per clock. This reduced command overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

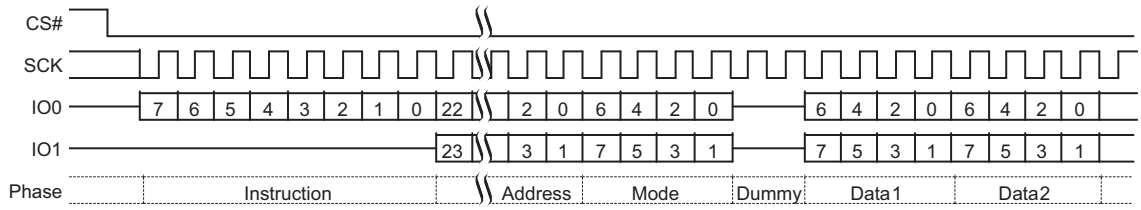
Fast Read Dual I/O with "Continuous Read Mode"

The Fast Read Dual I/O command can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 9.14. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O command through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O command (after CS# is raised and then lowered) does not require the BBh instruction code, as shown in Figure 9.15. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next command (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A "Continuous Read Mode" Reset command can also be used to reset (M7-0) before issuing normal commands (see See *Continuous Read Mode Reset (FFh or FFFFh)* on page 66.).

When variable read latency is enabled, the number of latency (Mode + Dummy) cycles is set by the Latency Control value in SR3 to optimize the latency for the frequency in use. See. Table 7.10, *Latency Cycles Versus Frequency* on page 49. Note that the legacy Read Dual I/O command has four Mode cycles and no Dummy cycles for a total of four latency cycles, Enabling the variable read latency allows for the addition of more read latency to enable higher frequency operation of the Dual I/O command.

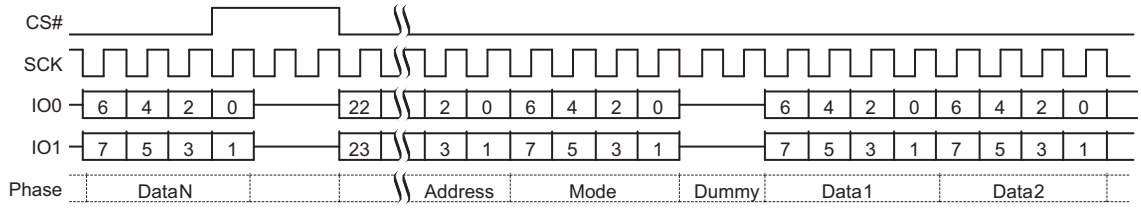
Figure 9.14 Fast Read Dual I/O Command Sequence (Initial command or previous M5-4 ≠ 10)



Note:

1. *Least significant 4 bits of Mode are don't care and it is optional for the host to drive these bits. The host may turn off drive during these cycles to increase bus turn around time between Mode bits from host and returning data from the memory.*

Figure 9.15 Fast Read Dual I/O Command Sequence (Previous command set M5-4 = 10)



9.3.6 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) command is similar to the Fast Read Dual I/O (BBh) command except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and four Dummy clock are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Command.

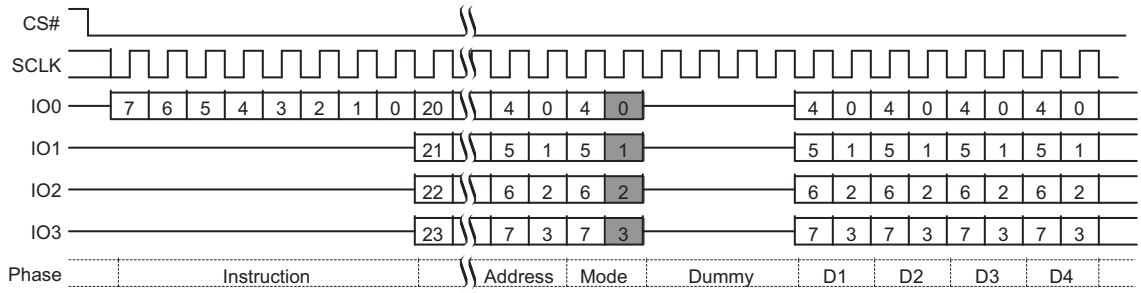
Fast Read Quad I/O with "Continuous Read Mode"

The Fast Read Quad I/O command can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 9.16, *Fast Read Quad I/O Command Sequence (Initial command or previous M5-4 ≠10)* on page 64. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O command through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O command (after CS# is raised and then lowered) does not require the EBh instruction code, as shown in Figure 9.17, *Fast Read Quad I/O Command Sequence (Previous command set M5-4 = 10)* on page 64. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next command (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A "Continuous Read Mode" Reset command can also be used to reset (M7-0) before issuing normal commands (see Section 9.3.8, *Continuous Read Mode Reset (FFh or FFFFh)* on page 66).

When variable read latency is enabled, the number of latency (Mode + Dummy) cycles is set by the Latency Control value in SR3 to optimize the latency for the frequency in use. See. Table 7.10, *Latency Cycles Versus Frequency* on page 49. Note that the legacy Read Quad I/O command has two Mode cycles plus four Dummy cycles for a total of six latency cycles, Enabling the variable read latency allows for the addition of more read latency to enable higher frequency operation of the Quad I/O command.

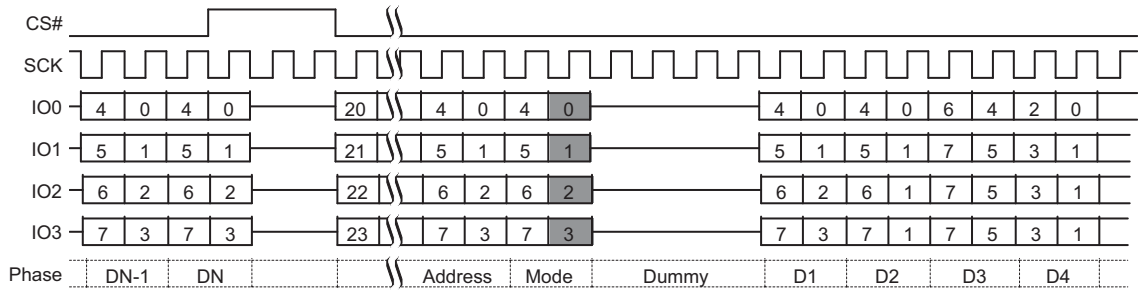
Figure 9.16 Fast Read Quad I/O Command Sequence (Initial command or previous M5-4 ≠10)



Note:

1. *Least significant 4 bits of Mode are don't care and it is optional for the host to drive these bits. The host may turn off drive during these cycles to increase bus turn around time between Mode bits from host and returning data from the memory.*

Figure 9.17 Fast Read Quad I/O Command Sequence (Previous command set M5-4 = 10)



Fast Read Quad I/O with "16/32/64-Byte Wrap Around"

The Fast Read Quad I/O command can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" command prior to EBh. The "Set Burst with Wrap" command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either a 16/32/64-byte section of data. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (16/32/64-bytes) of data without issuing multiple read commands.

The "Set Burst with Wrap" command allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See Section 9.3.7, *Set Burst with Wrap (77h)* on page 65.

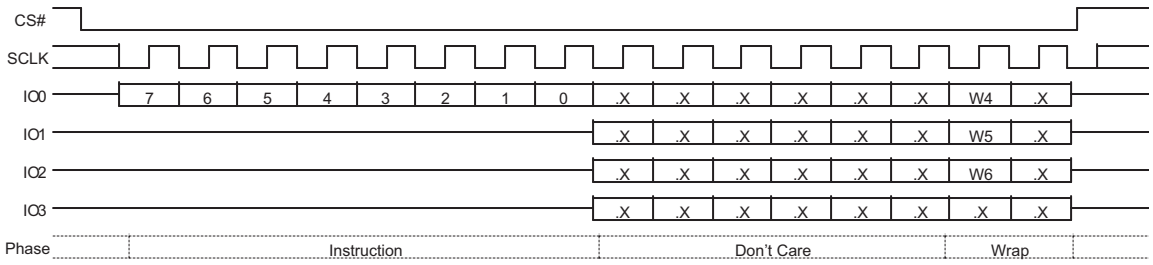
9.3.7 Set Burst with Wrap (77h)

The Set Burst with Wrap (77h) command is used in conjunction with "Fast Read Quad I/O" commands to access a fixed length and alignment of 8/16/32/64-bytes of data. Certain applications can benefit from this feature and improve the overall system code execution performance. This command loads the SR3 bits.

Similar to a Quad I/O command, the Set Burst with Wrap command is initiated by driving the CS# pin low and then shifting the instruction code "77h" followed by 24-dummy bits and 8 "Wrap Bits", W7-0. The command sequence is shown in Figure 9.18, *Set Burst with Wrap Command Sequence* on page 65. Wrap bit W7 and the lower nibble W3-0 are not used. See Status Register-3 (SR3[6:4]) for the encoding of W6-W4 in Section 7.4, *Status Registers* on page 43.

Once W6-4 is set by a Set Burst with Wrap command, all the following "Fast Read Quad I/O" commands will use the W6-4 setting to access the 8/16/32/64-byte section of data. Note, Status Register-2 QE bit (SR2[1]) must be set to 1 in order to use the Fast Read Quad I/O and Set Burst with Wrap commands. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4 = 1. The default value of W4 upon power on is 1. In the case of a system Reset while W4 = 0, it is recommended that the controller issues a Set Burst with Wrap command to reset W4 = 1 prior to any normal Read commands since S25FL116K does not have a hardware Reset Pin.

Figure 9.18 Set Burst with Wrap Command Sequence



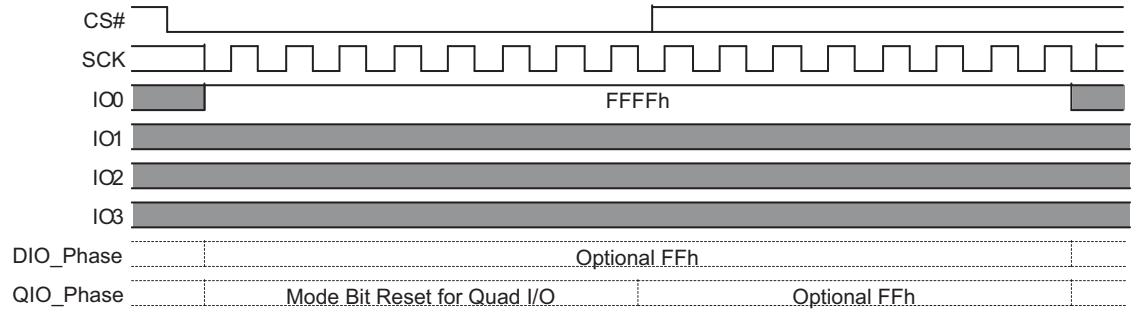
9.3.8 Continuous Read Mode Reset (FFh or FFFFh)

The “Continuous Read Mode” bits are used in conjunction with “Fast Read Dual I/O” and “Fast Read Quad I/O” commands to provide the highest random flash memory access rate with minimum SPI instruction overhead, thus allowing more efficient XIP (execute in place) with this device family.

The “Continuous Read Mode” bits M7-0 are set by the Dual/Quad I/O Read commands. M5-4 are used to control whether the 8-bit SPI instruction code (BBh or EBh) is needed or not for the next command. When M5-4 = (1,0), the next command will be treated the same as the current Dual/Quad I/O Read command without needing the 8-bit instruction code; when M5-4 do not equal to (1,0), the device returns to normal SPI command mode, in which all commands can be accepted. M7-6 and M3-0 are reserved bits for future use, either 0 or 1 values can be used.

The Continuous Read Mode Reset command (FFh or FFFFh) can be used to set M4 = 1, thus the device will release the Continuous Read Mode and return to normal SPI operation, as shown in Figure 9.19.

Figure 9.19 Continuous Read Mode Reset for Fast Read Dual or Quad I/O



Notes:

1. *To reset “Continuous Read Mode” during Quad I/O operation, only eight clocks are needed. The instruction is “FFh”.*
2. *To reset “Continuous Read Mode” during Dual I/O operation, sixteen clocks are needed to shift in instruction “FFFFh”.*

9.3.9 Host System Reset Commands.

Since S25FL116K does not have a hardware Reset pin, if the host system memory controller resets, without a complete power down and power up sequence, while an S25FL116K device is set to Continuous Mode Read, the S25FL116K device will not recognize any initial standard SPI commands from the controller. To address this possibility, it is recommended to issue a Continuous Read Mode Reset (FFFFh) command as the first command after a system Reset. Doing so will release the device from the Continuous Read Mode and allow Standard SPI commands to be recognized. See Section 9.3.8, *Continuous Read Mode Reset (FFh or FFFFh)* on page 66

If Burst Wrap Mode is used, it is also recommended to issue a Set Burst with Wrap (77h) command that sets the W4 bit to one as the second command after a system Reset. Doing so will release the device from the Burst Wrap Mode and allow standard sequential read SPI command operation. See Section 9.3.7, *Set Burst with Wrap (77h)* on page 65.

Issuing these commands immediately after a non-power-cycle (warm) system reset, ensures the device operation is consistent with the power on default device operation. The same commands may also be issued after device power on (cold) reset so that system reset code is the same for warm or cold reset.

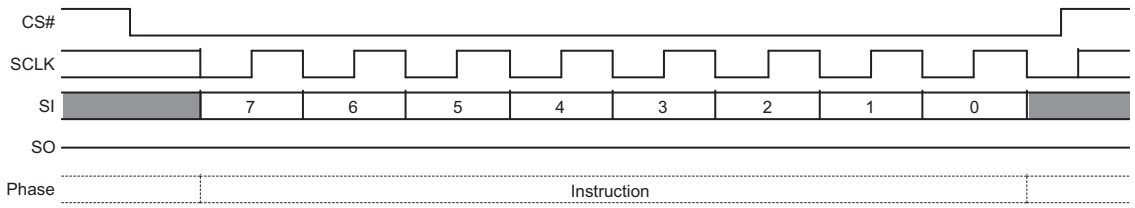
9.4 ID and Security Commands

9.4.1 Deep-Power-Down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep-Power-Down command. The lower power consumption makes the Deep-Power-Down (DPD) command especially useful for battery powered applications (see I_{CC1} and I_{CC2} in Section 5.7, *AC Electrical Characteristics* on page 30). The command is initiated by driving the CS# pin low and shifting the instruction code “B9h” as shown in Figure 9.20.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Deep-Power-Down command will not be executed. After CS# is driven high, the power-down state will entered within the time duration of t_{DP} (Section 5.7, *AC Electrical Characteristics* on page 30). While in the power-down state only the Release from Deep-Power-Down / Device ID command, which restores the device to normal operation, will be recognized. All other commands are ignored. This includes the Read Status Register command, which is always available during normal operation. Ignoring all but one command also makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of I_{CC1}.

Figure 9.20 Deep Power-Down Command Sequence



9.4.2 Release from Deep-Power-Down / Device ID (ABh)

The Release from Deep-Power-Down / Device ID command is a multi-purpose command. It can be used to release the device from the deep-power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the deep-power-down state, the command is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high as shown in Figure 9.21. Release from deep-power-down will take the time duration of t_{RES1} (Section 5.7, *AC Electrical Characteristics* on page 30) before the device will resume normal operation and other commands are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the deep power-down state, the command is initiated by driving the CS# pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first. The Device ID values for the S25FL116K is listed in Section 7.5.1, *Legacy Device Identification Commands* on page 50. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the deep-power-down state and obtain the Device ID, the command is the same as previously described, and shown in Figure 9.22, except that after CS# is driven high it must remain high for a time duration of t_{RES2}. After this time duration the device will resume normal operation and other commands will be accepted. If the Release from Deep-Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the command is ignored and will not have any effects on the current cycle.

Figure 9.21 Release from Deep-Power-Down Command Sequence

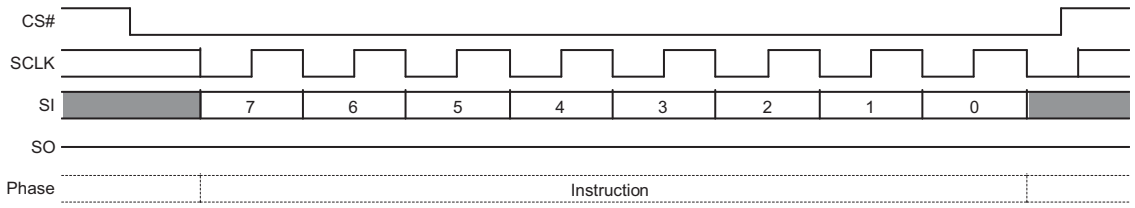
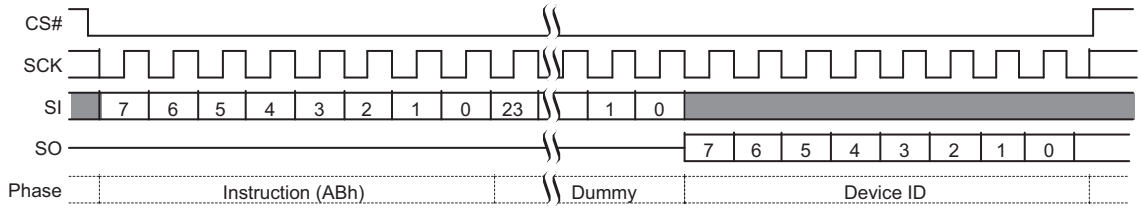


Figure 9.22 Read Electronic Signature (RES ABh) Command Sequence

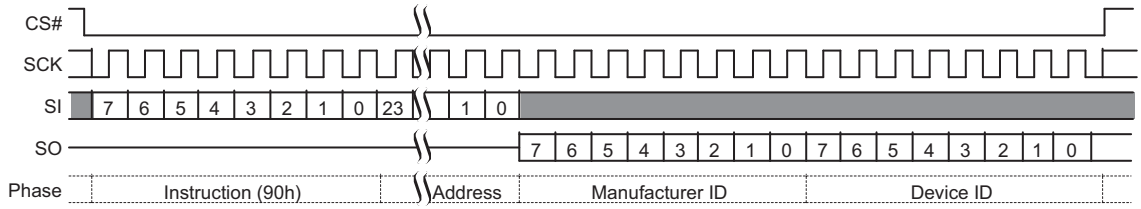


9.4.3 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID command is an alternative to the Release from Deep-Power-Down / Device ID command that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID command is very similar to the Release from Deep-Power-Down / Device ID command. The command is initiated by driving the CS# pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 9.23. The Device ID values for the S25FL116K is listed in Section 7.5.1, *Legacy Device Identification Commands* on page 50. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The command is completed by driving CS# high.

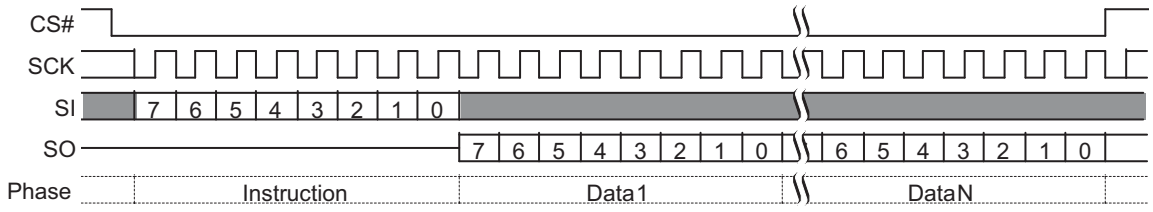
Figure 9.23 READ_ID (90h) Command Sequence



9.4.4 Read JEDEC ID (9Fh)

For compatibility reasons, the S25FL116K provides several commands to electronically determine the identity of the device. The Read JEDEC ID command is compatible with the JEDEC standard for SPI compatible serial flash memories that was adopted in 2003. The command is initiated by driving the CS# pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 9.24. For memory type and capacity values refer to Section 7.5.1, *Legacy Device Identification Commands* on page 50.

Figure 9.24 Read JEDEC ID Command Sequence

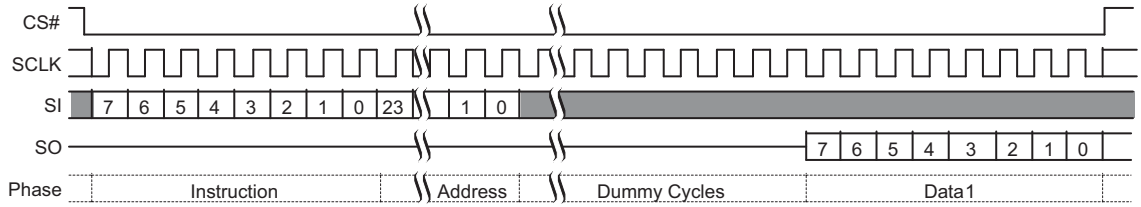


9.4.5 Read SFDP Register (5Ah)

The Read SFDP command is initiated by driving the CS# pin low and shifting the instruction code “5Ah” followed by a 24-bit address (A23-A0) into the SI pin. Eight “dummy” clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 9.25. For SFDP register values and descriptions, refer to Table 7.3, *Serial Flash Discoverable Parameter Definition Table* on page 41.

Note: A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-byte SFDP Register.

Figure 9.25 Read SFDP Register Command Sequence



9.4.6 Erase Security Registers (44h)

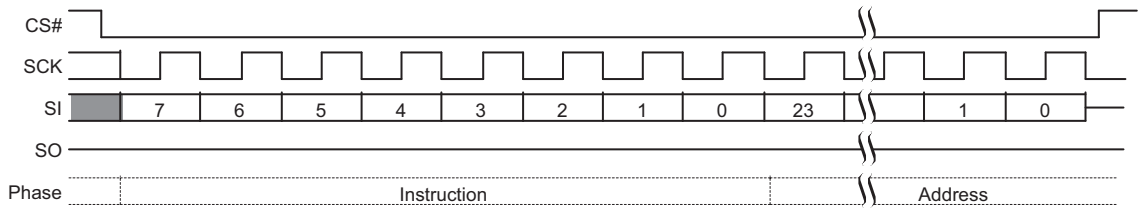
The Erase Security Register command is similar to the Sector Erase command. A Write Enable command must be executed before the device will accept the Erase Security Register Command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the instruction code “44h” followed by a 24-bit address (A23-A0) to erase one of the security registers.

Address	A23-16	A15-8	A7-0
Security Register-1	00h	10h	xxh
Security Register-2	00h	20h	xxh
Security Register-3	00h	30h	xxh

Note:
1. Addresses outside the ranges in the table have undefined results.

The Erase Security Register command sequence is shown in Figure 9.26. The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the command will not be executed. After CS# is driven high, the self-timed Erase Security Register operation will commence for a time duration of t_{SE} (see Section 5.7, *AC Electrical Characteristics* on page 30). While the Erase Security Register cycle is in progress, the Read Status Register command may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3:1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, and an Erase Security Register command to that register will be ignored (see *Security Register Lock Bits (LB3, LB2, LB1, LB0)* on page 48).

Figure 9.26 Erase Security Registers Command Sequence



9.4.7 Program Security Registers (42h)

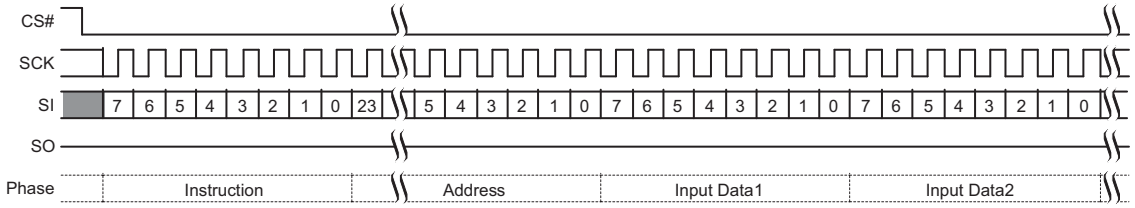
The Program Security Register command is similar to the Page Program command. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable command must be executed before the device will accept the Program Security Register Command (Status Register bit WEL= 1). The command is initiated by driving the CS# pin low then shifting the instruction code “42h” followed by a 24-bit address (A23-A0) and at least one data byte, into the SI pin. The CS# pin must be held low for the entire length of the command while data is being sent to the device.

Address	A23-16	A15-8	A7-0
Security Register-1	00h	10h	Byte Address
Security Register-2	00h	20h	Byte Address
Security Register-3	00h	30h	Byte Address

Note:
1. Addresses outside the ranges in the table have undefined results.

The Program Security Register command sequence is shown in Figure 9.27. The Security Register Lock Bits (LB3:1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, and a Program Security Register command to that register will be ignored (see *Security Register Lock Bits (LB3, LB2, LB1, LB0)* on page 48 and *Page Program (02h)* on page 58 for detail descriptions).

Figure 9.27 Program Security Registers Command Sequence



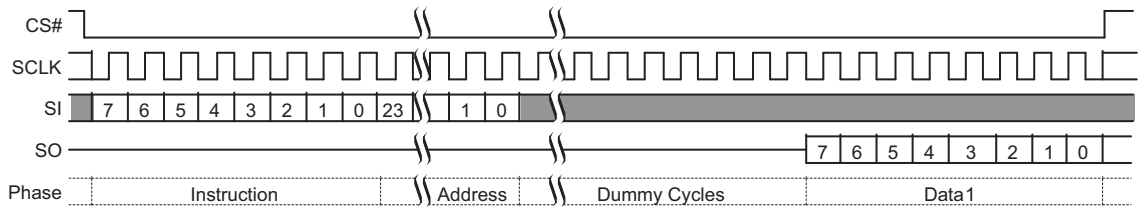
9.4.8 Read Security Registers (48h)

The Read Security Register command is similar to the Fast Read command and allows one or more data bytes to be sequentially read from one of the three security registers. The command is initiated by driving the CS# pin low and then shifting the instruction code “48h” followed by a 24-bit address (A23-A0) and eight “dummy” clocks into the SI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, and following the eight dummy cycles, the data byte of the addressed memory location will be shifted out on the SO pin at the falling edge of CLK with most significant bit (MSB) first. Locations with address bits A23-A16 not equal to zero, have undefined data. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte FFh), it will reset to 00h, the first byte of the register, and continue to increment. The command is completed by driving CS# high. The Read Security Register command sequence is shown in Figure 9.28. If a Read Security Register command is issued while an Erase, Program, or Write cycle is in process (BUSY=1), the command is ignored and will not have any effects on the current cycle. The Read Security Register command allows clock rates from DC to a maximum of F_R (see Section 5.7, *AC Electrical Characteristics* on page 30).

Address	A23-16	A15-8	A7-0
Security Register-0 (SFDP)	00h	00h	Byte Address
Security Register-1	00h	10h	Byte Address
Security Register-2	00h	20h	Byte Address
Security Register-3	00h	30h	Byte Address

Note:
1. *Addresses outside the ranges in the table have undefined results.*

Figure 9.28 Read Security Registers Command Sequence



10. Data Integrity

10.1 Endurance

The Joint Electron Device Engineering Council (JEDEC) standard JESD22-A117 defines the procedural requirements for performing valid endurance and retention tests based on a qualification specification. This methodology is intended to determine the ability of a flash device to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life (data retention). Endurance and retention qualification specifications are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.

10.1.1 Erase Endurance

Table 10.1 Erase Endurance

Parameter	Min	Typical	Unit
Erase per sector	100K		cycle

Note:
1. Data retention of 20 years is based on 1K erase cycles or less.

10.2 Initial Delivery State

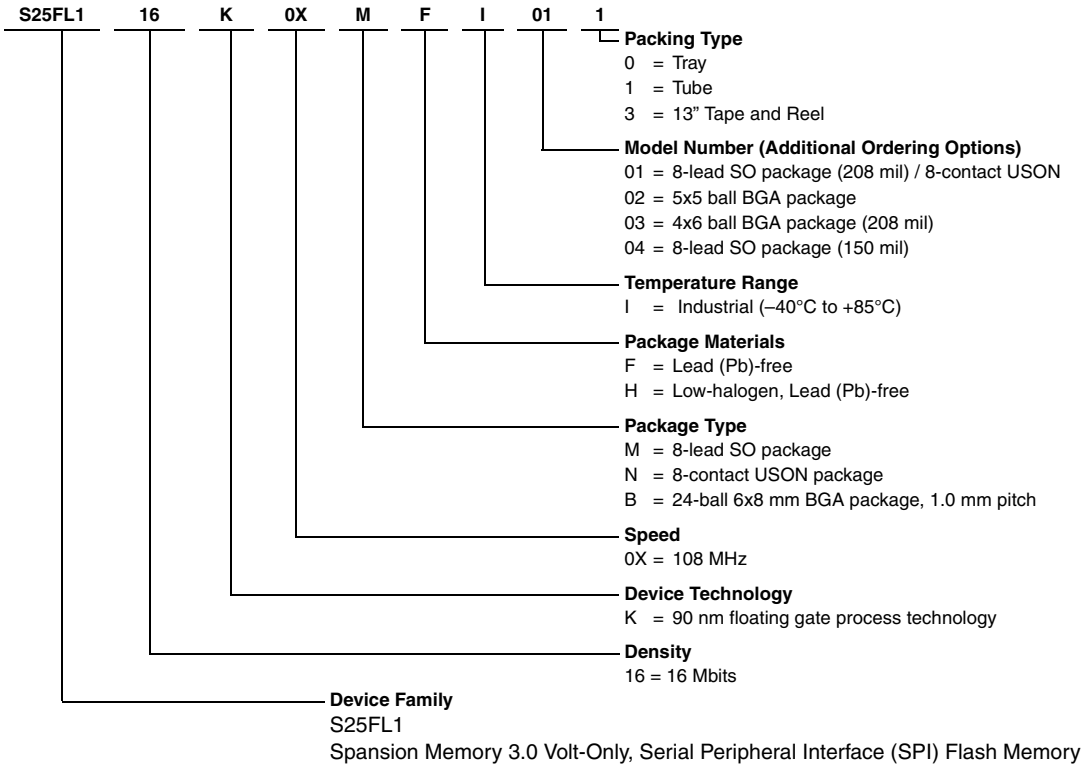
The device is shipped from Spansion with non-volatile bits / default states set as follows:

- The entire memory array is erased: i.e. all bits are set to 1 (each byte contains FFh).
- The Unique Device ID is programmed to a random number seeded by the date and time of device test.
- The SFDP Security Register address space 0 contains the values as defined in Table 7.3, *Serial Flash Discoverable Parameter Definition Table* on page 41. Security Register address spaces 1 to 3 are erased: i.e. all bits are set to 1 (each byte contains FFh).
- Status Register-1 contains 00h.
- Status Register-2 contains 04h.
- Status Register-3 contains 70h

Ordering Information

11. Ordering Part Number

The ordering part number is formed by a valid combination of the following:



11.1 Valid Combinations

The valid combinations supported for this family.

Table 11.1 Valid Combinations

Base Ordering Part Number	Speed Option	Package and Temperature	Model Number	Packing Type	Package Marking
FL116K	0X	MFI	01	0, 1, 3	FL116KIF01
			04		FL116KIF4
		NFI	01		FL116KIF01
		BHI	02	0, 3	FL116KIH02
			03		FL116KIH03

12. Contacting Spansion

Obtain the latest list of company locations and contact information at

http://www.spansion.com/About/Pages/Locations.aspx

13. Revision History

Section	Description
Revision 01 (January 11, 2013)	
	Initial release
Revision 02 (April 10, 2013)	
Features	Updated Cycling Endurance information
DC Electrical Characteristics	Updated the typical value of I_{CC1} and added Max values for I_{CC1} and I_{CC2}
AC Electrical Characteristics	Updated Write Status Registers Time and Block Erase Time values
Data Integrity	Added a paragraph Updated Erase Endurance information Removed Data Retention section

Colophon

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